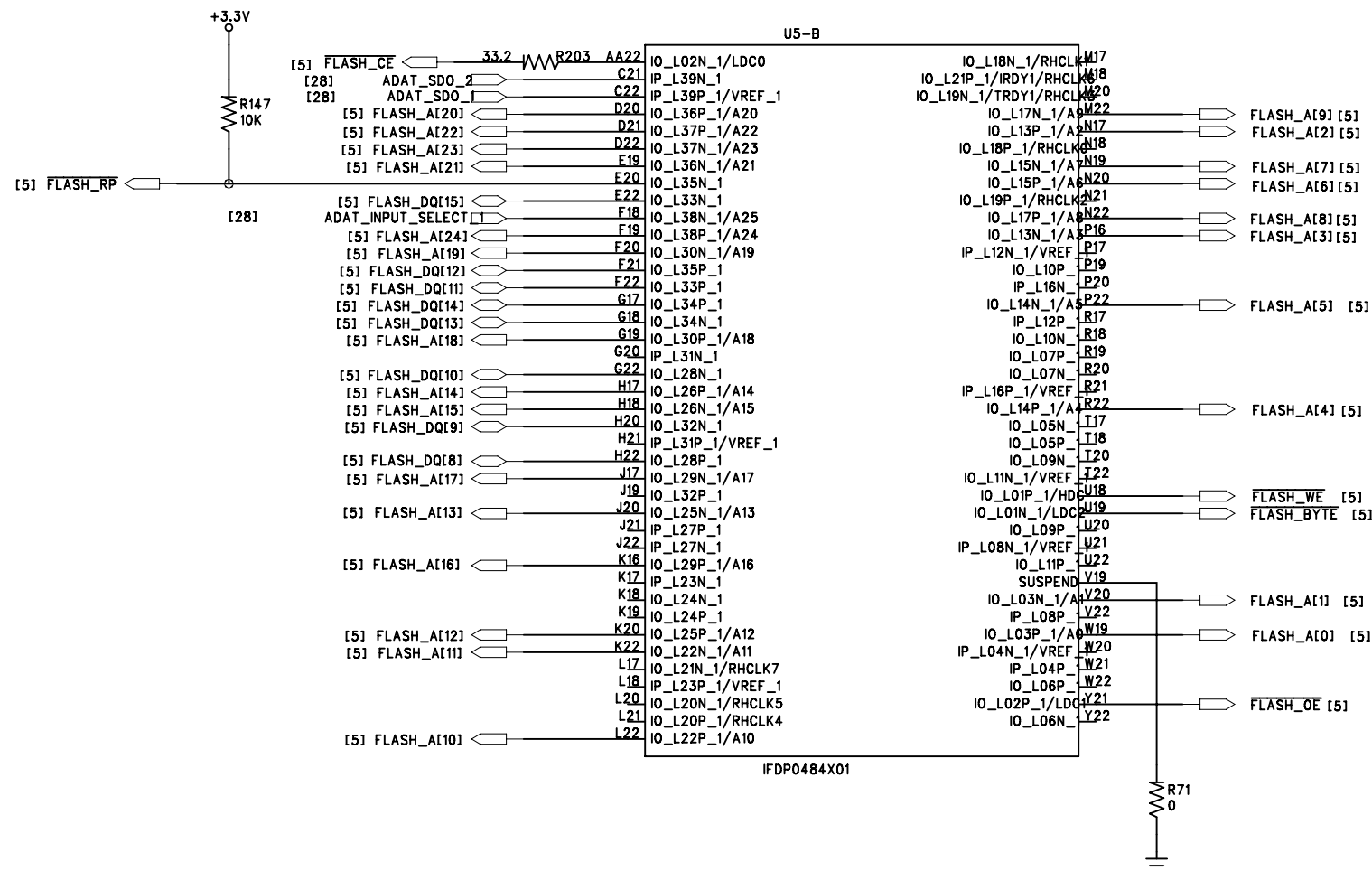
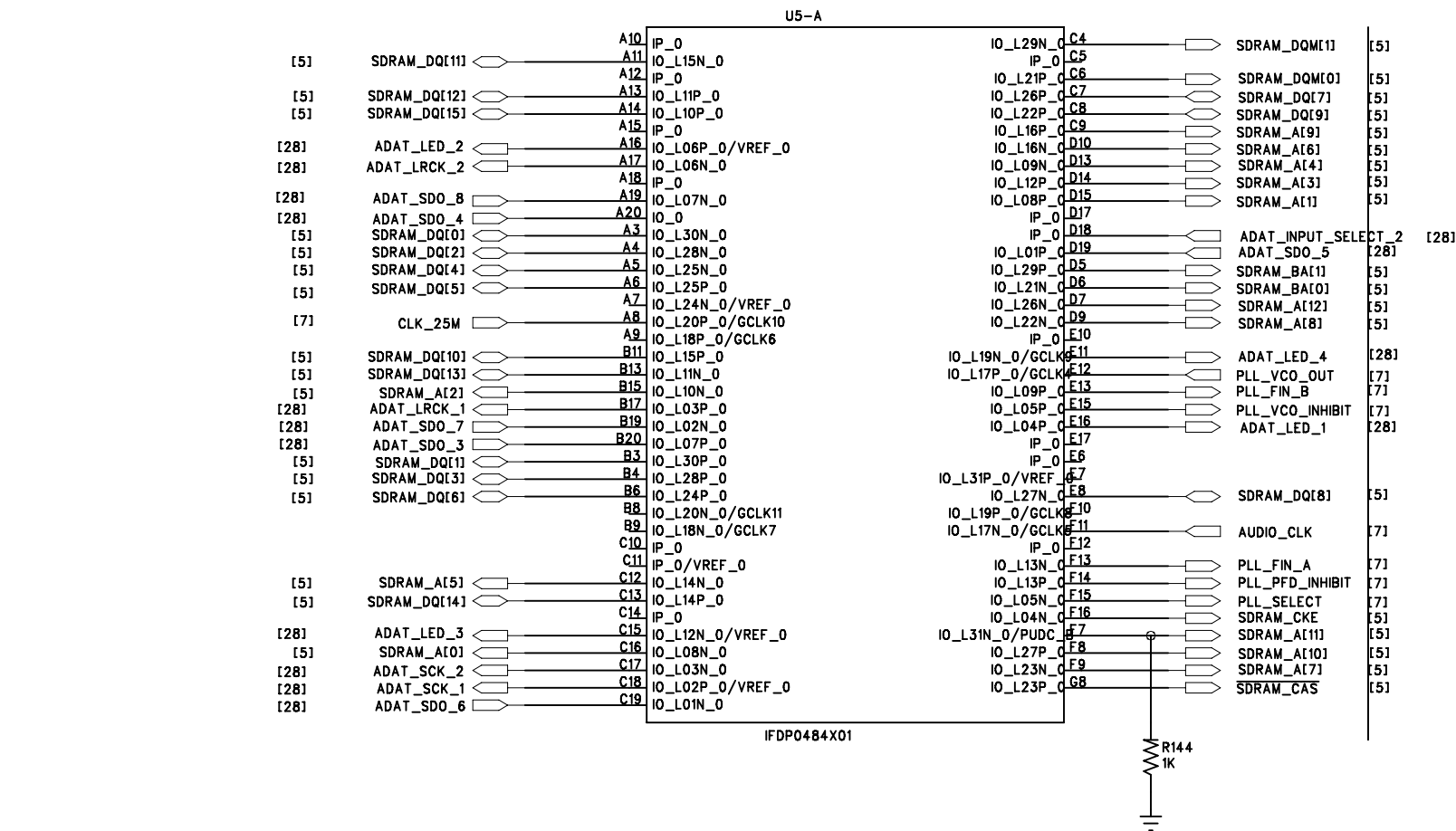


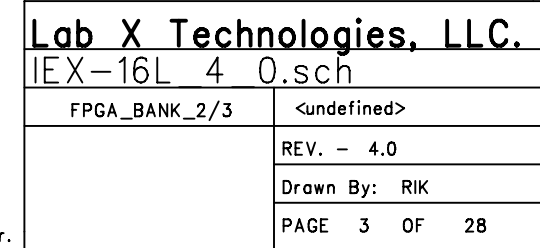
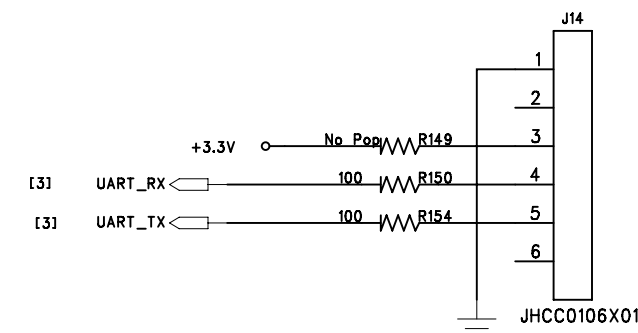
Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
TITLE_PAGE	<undefined>
	REV. - 4.0
	Drawn By: RIK
	PAGE 1 OF 28

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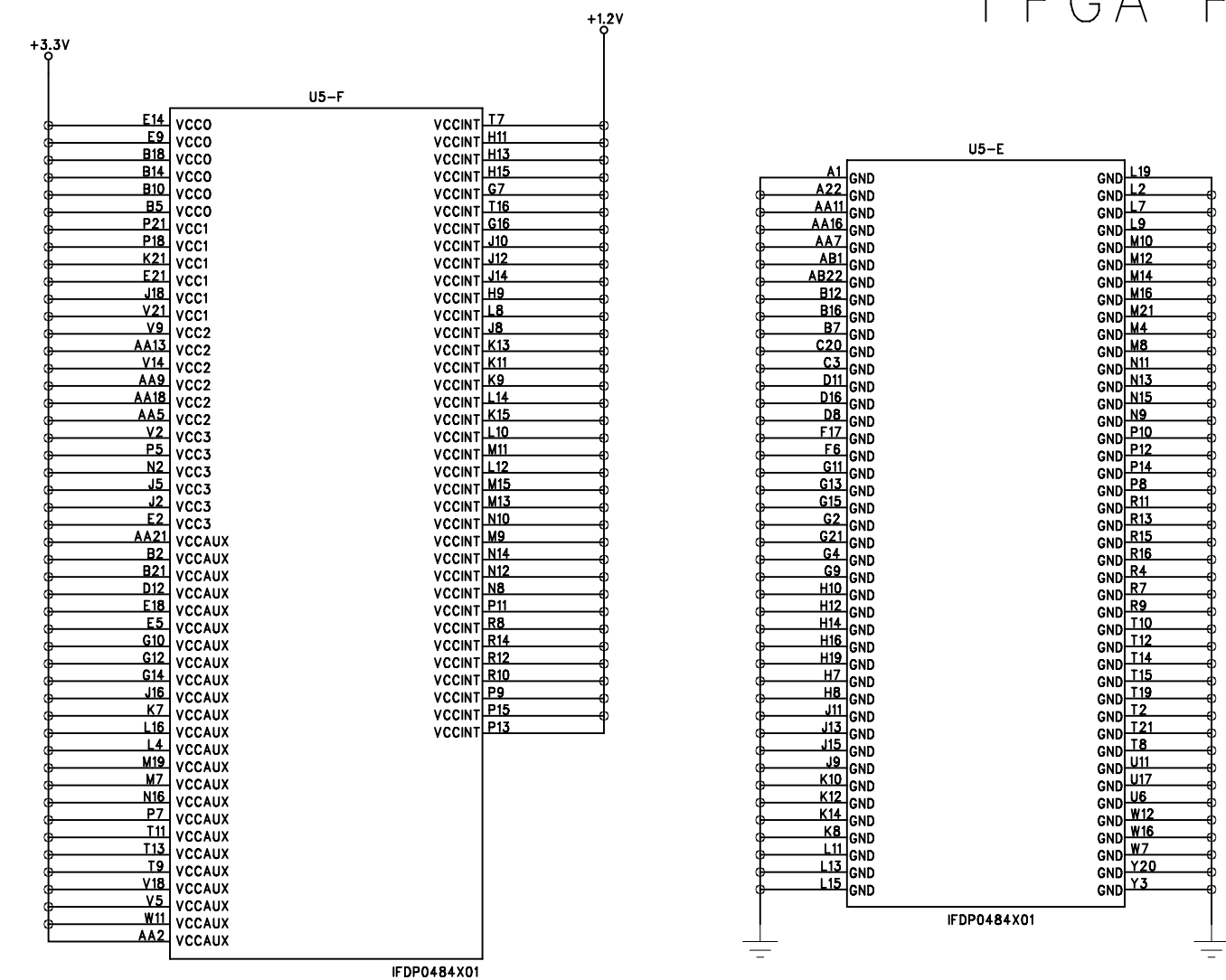
Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
FPGA_BANK_0/1	<undefined>
	REV. - 4.0
	Drawn By: RIK
	PAGE 2 OF 28

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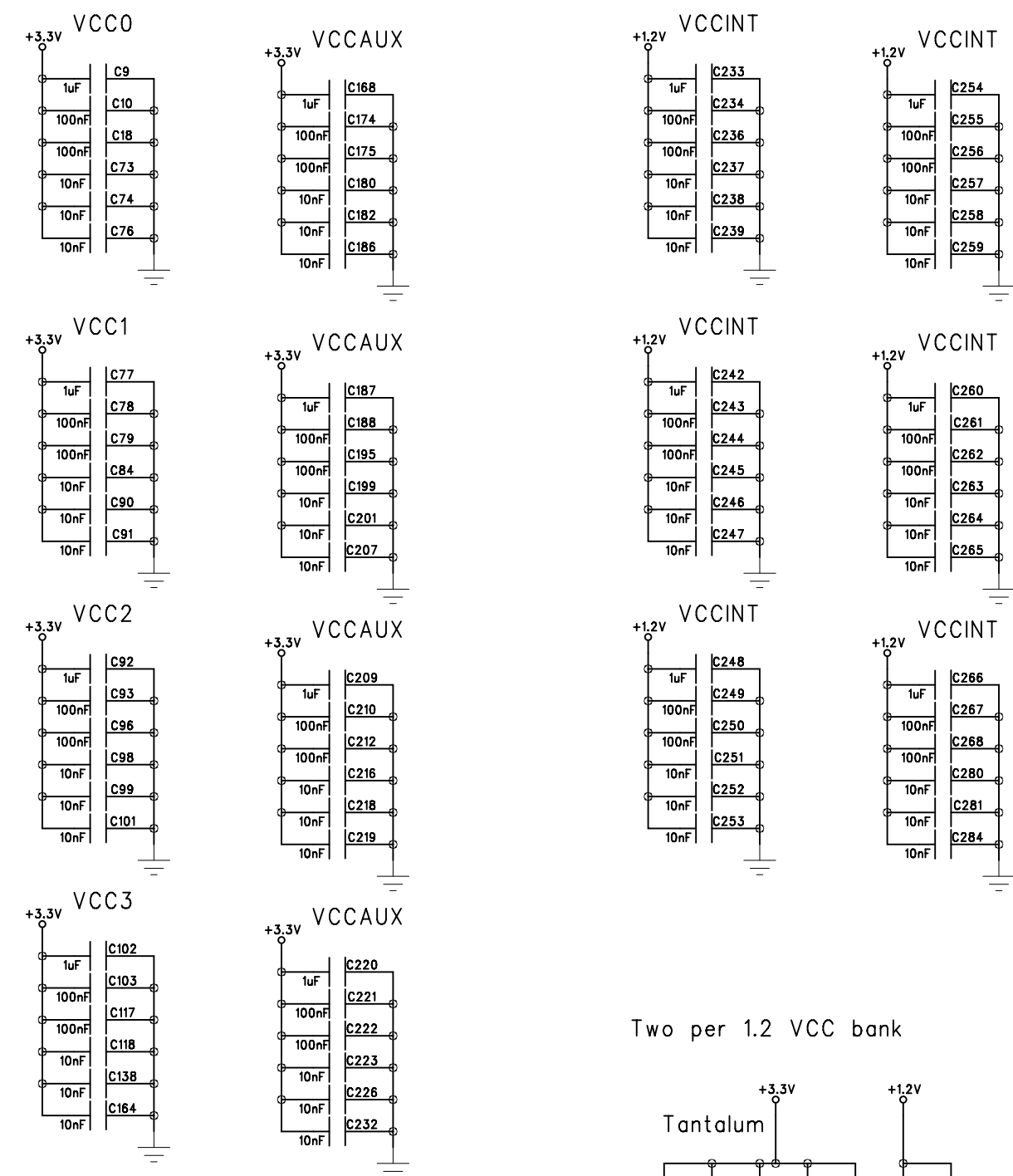


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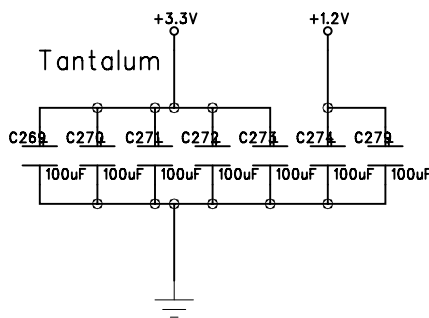
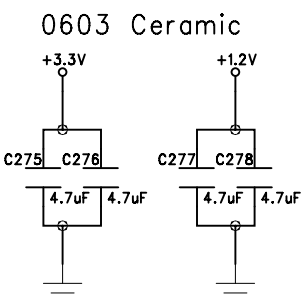
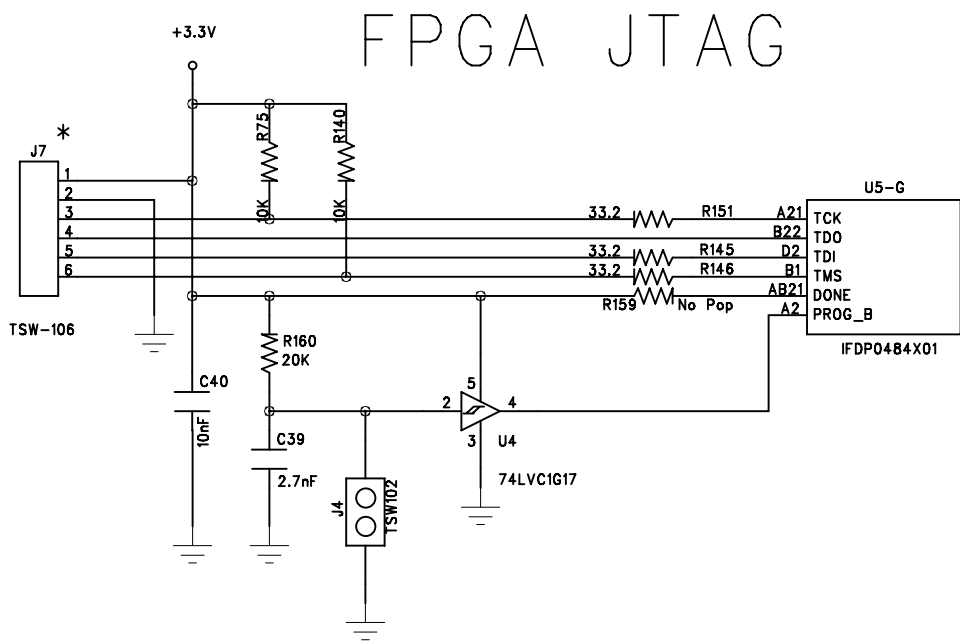
FPGA Power and Ground



0402 Ceramic



Two per 1.2 VCC bank



Lab X Technologies, LLC.

LEX-16L 4 0.sch

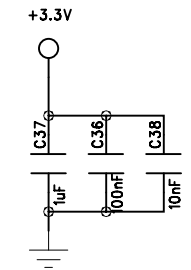
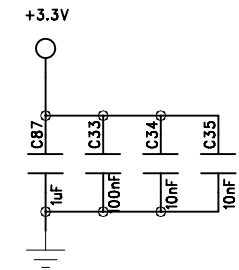
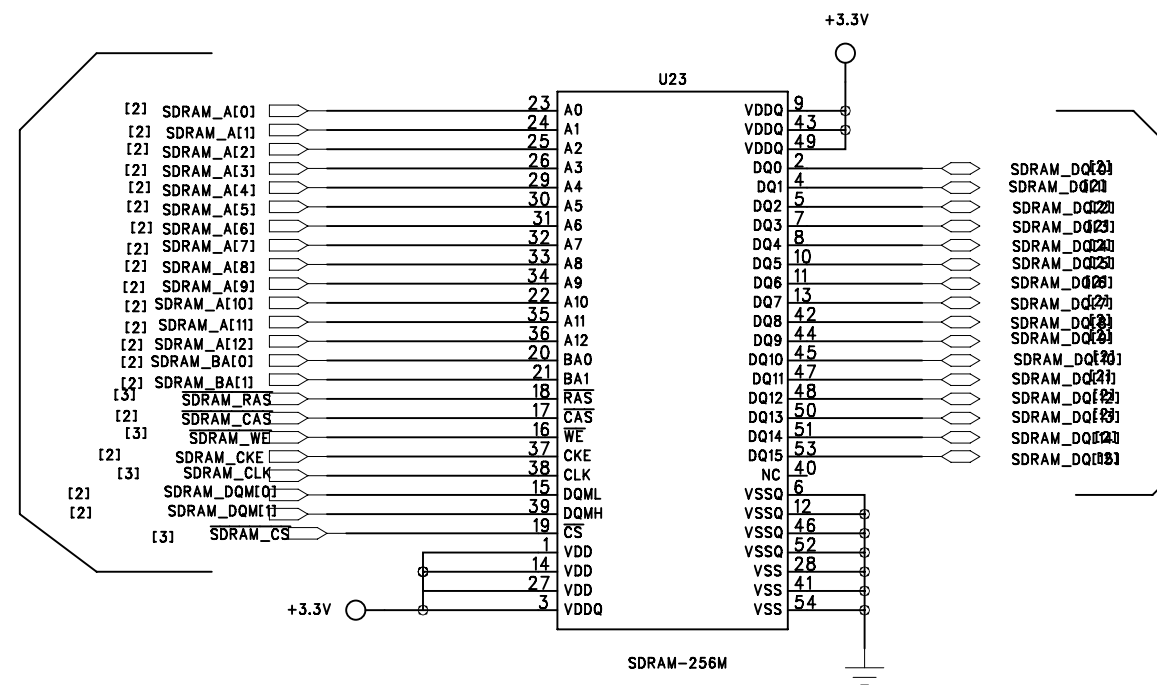
POWER-GATES <undefined>

REV. - 4.0

Drawn By: RIK

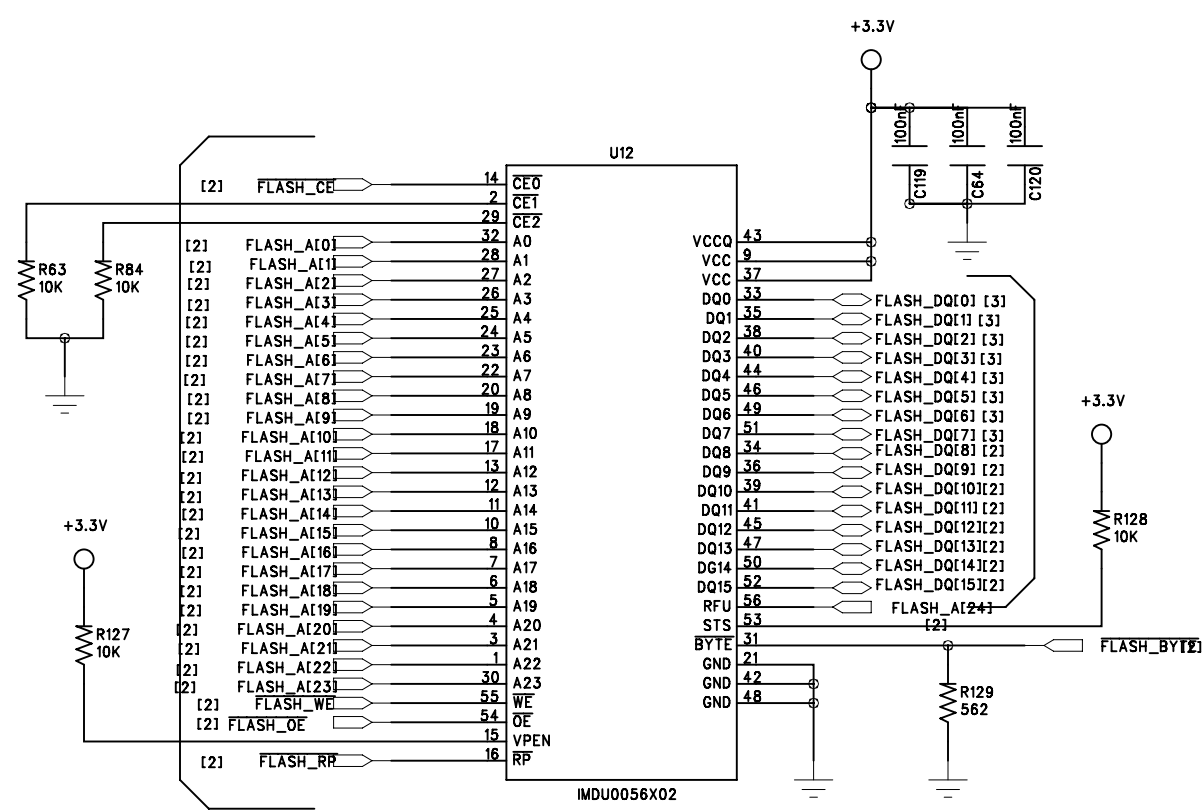
PAGE 4 OF 28

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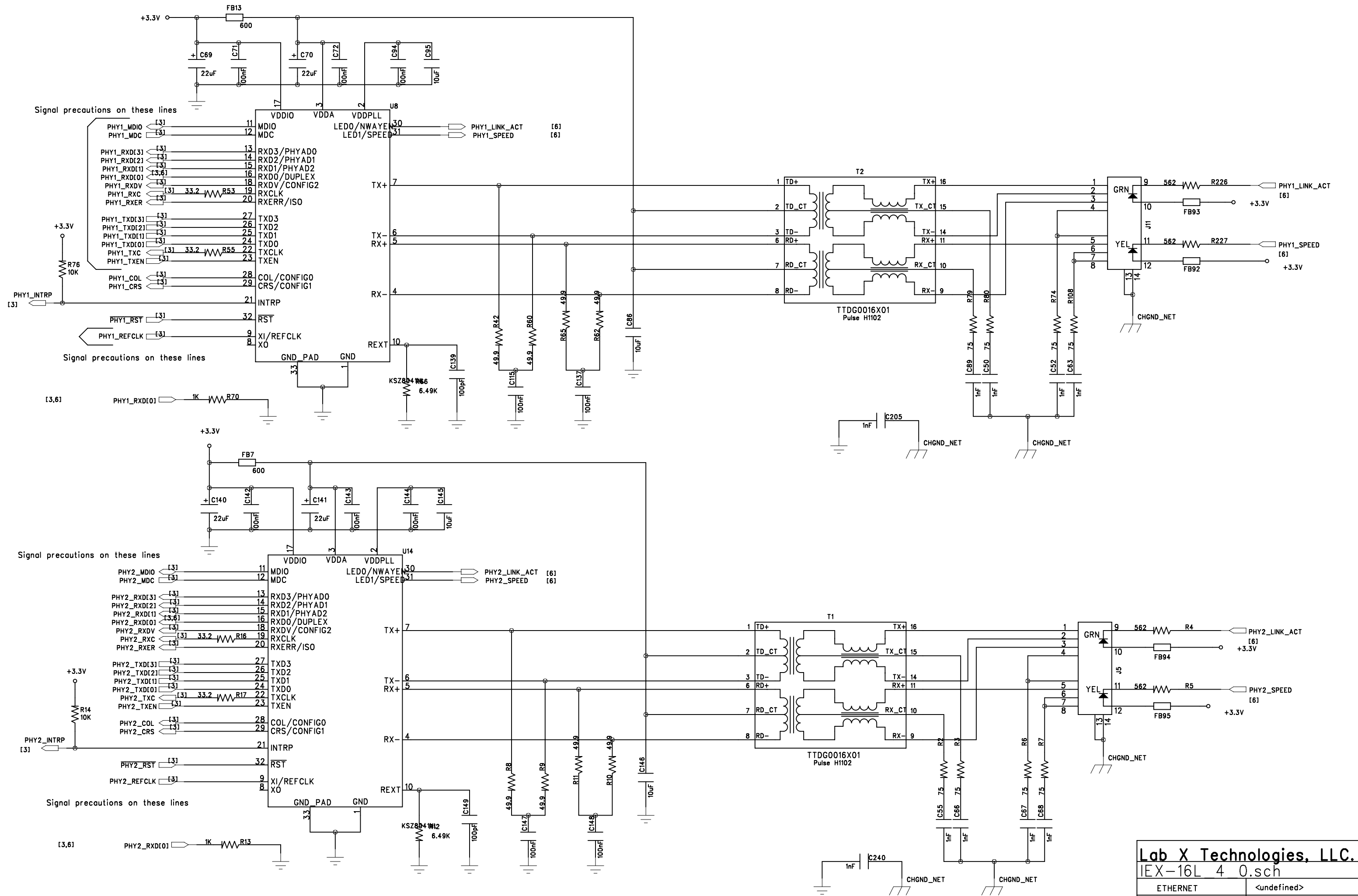
Minimize vias.
Keep on inner layer whenever possible.
Drop a ground via anywhere these signals have a via transition.

Check voltages after the flash chip change



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IEX-16L 4 0.sch	
SDRAM_FLASH	<undefined>
REV. - 4.0	
Drawn By: RIK	
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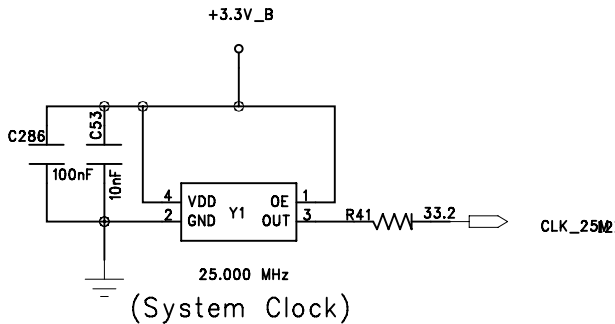
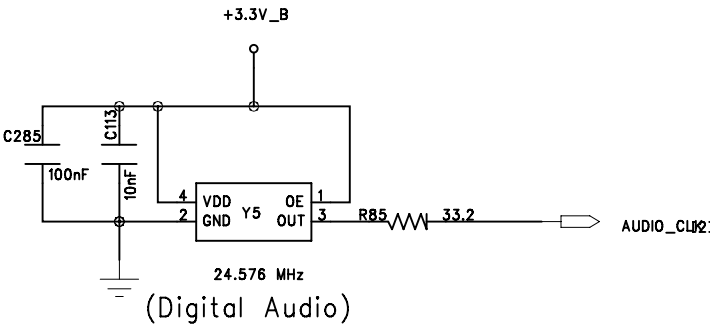
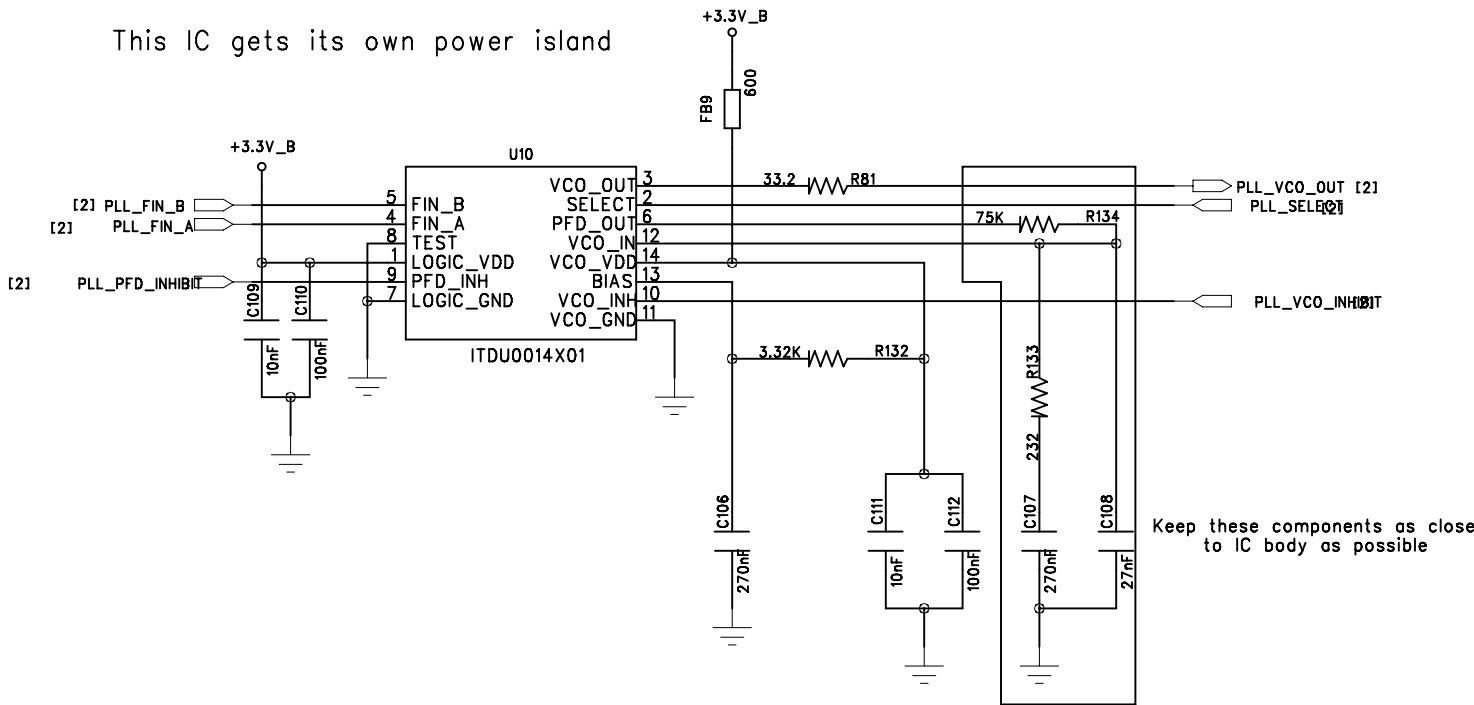


Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
ETHERNET	<undefined>
REV. - 4.0	
Drawn By: RIK	
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Very clean layout of these traces!!!!

This IC gets its own power island



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LEX-16L 4 0.sch

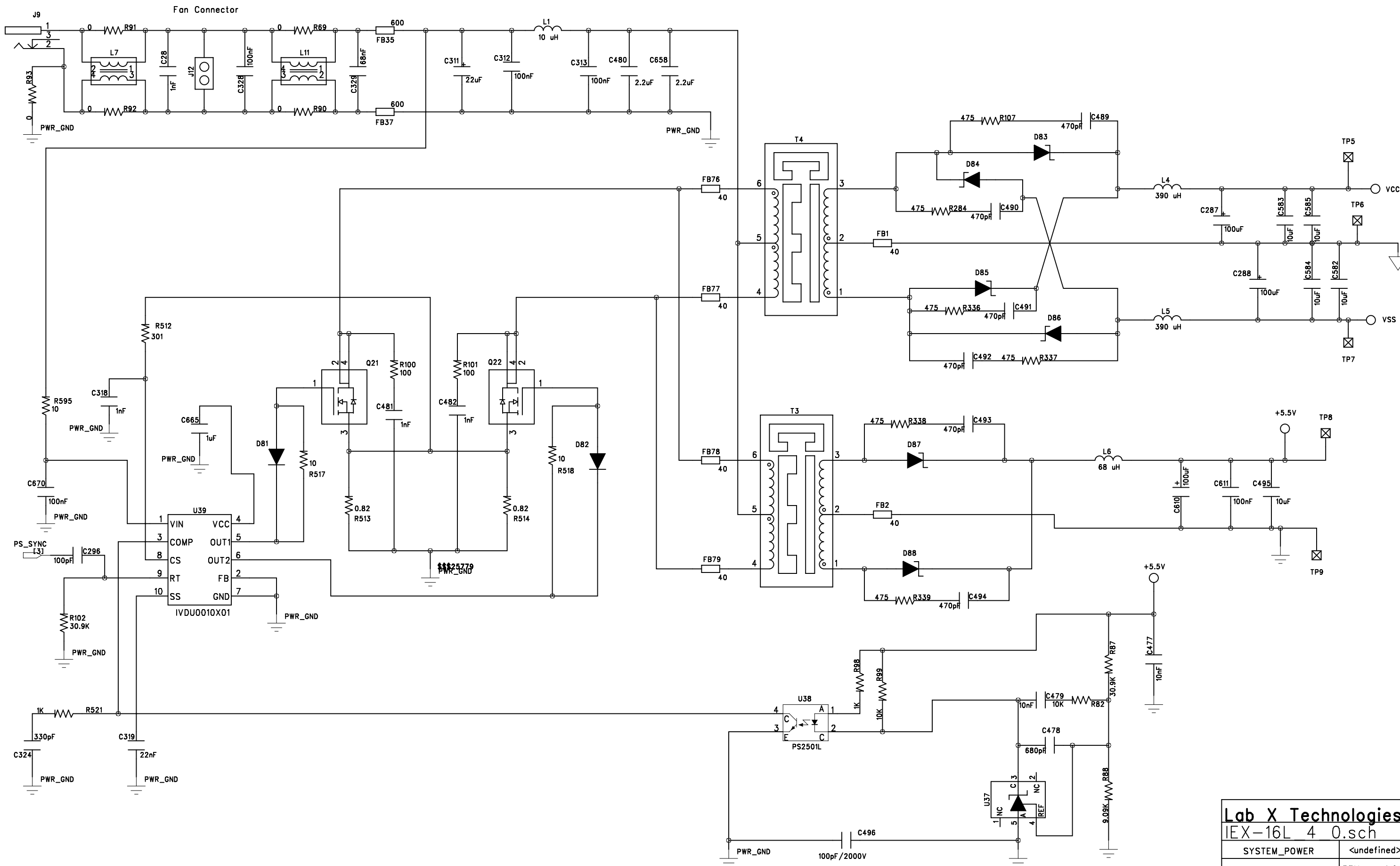
PLL <undefined>

REV. - 4.0

Drawn By: RIK

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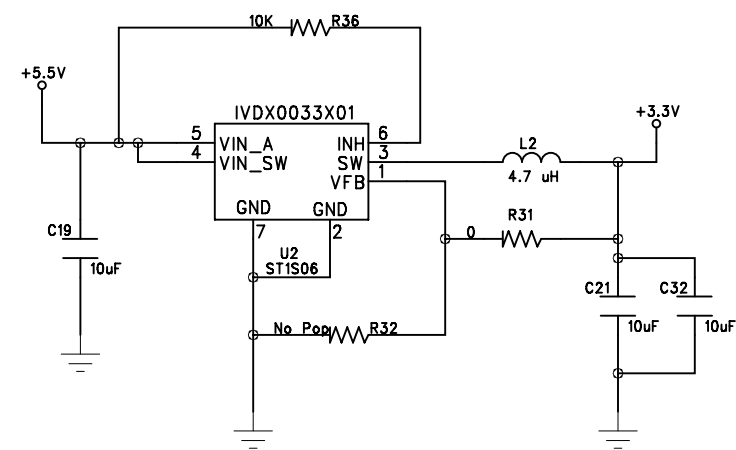
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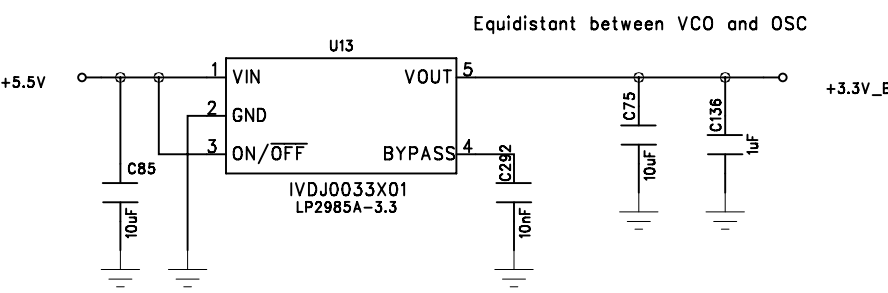
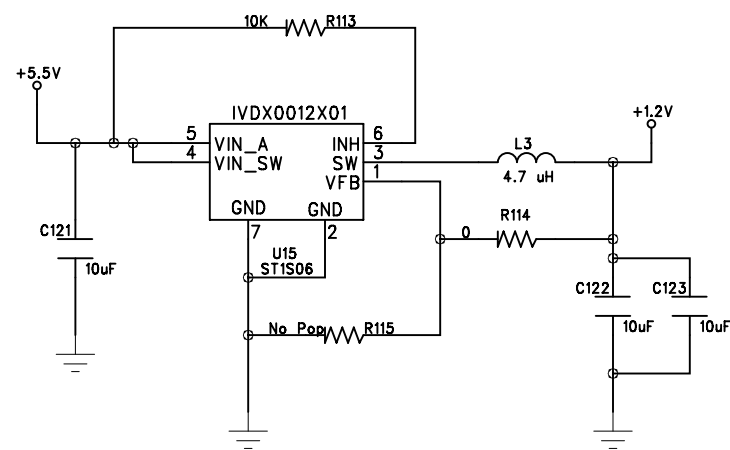
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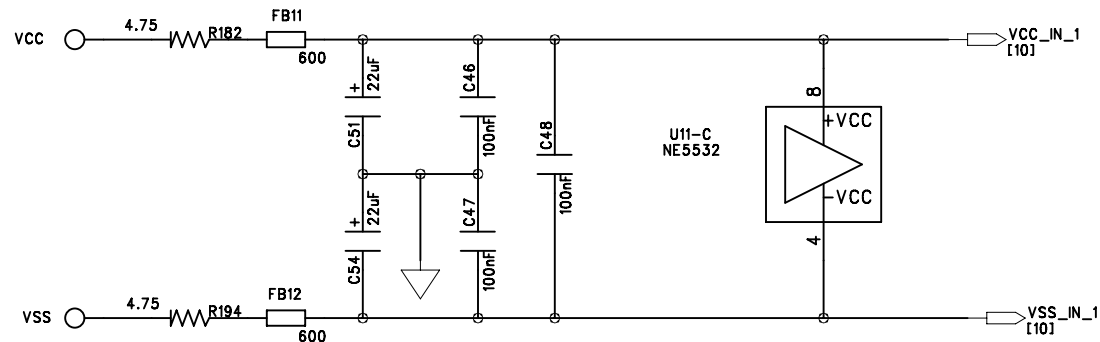
Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
SYSTEM_POWER	<undefined>
REV. - 4.0	
Drawn By: RIK	
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3.3V Supply

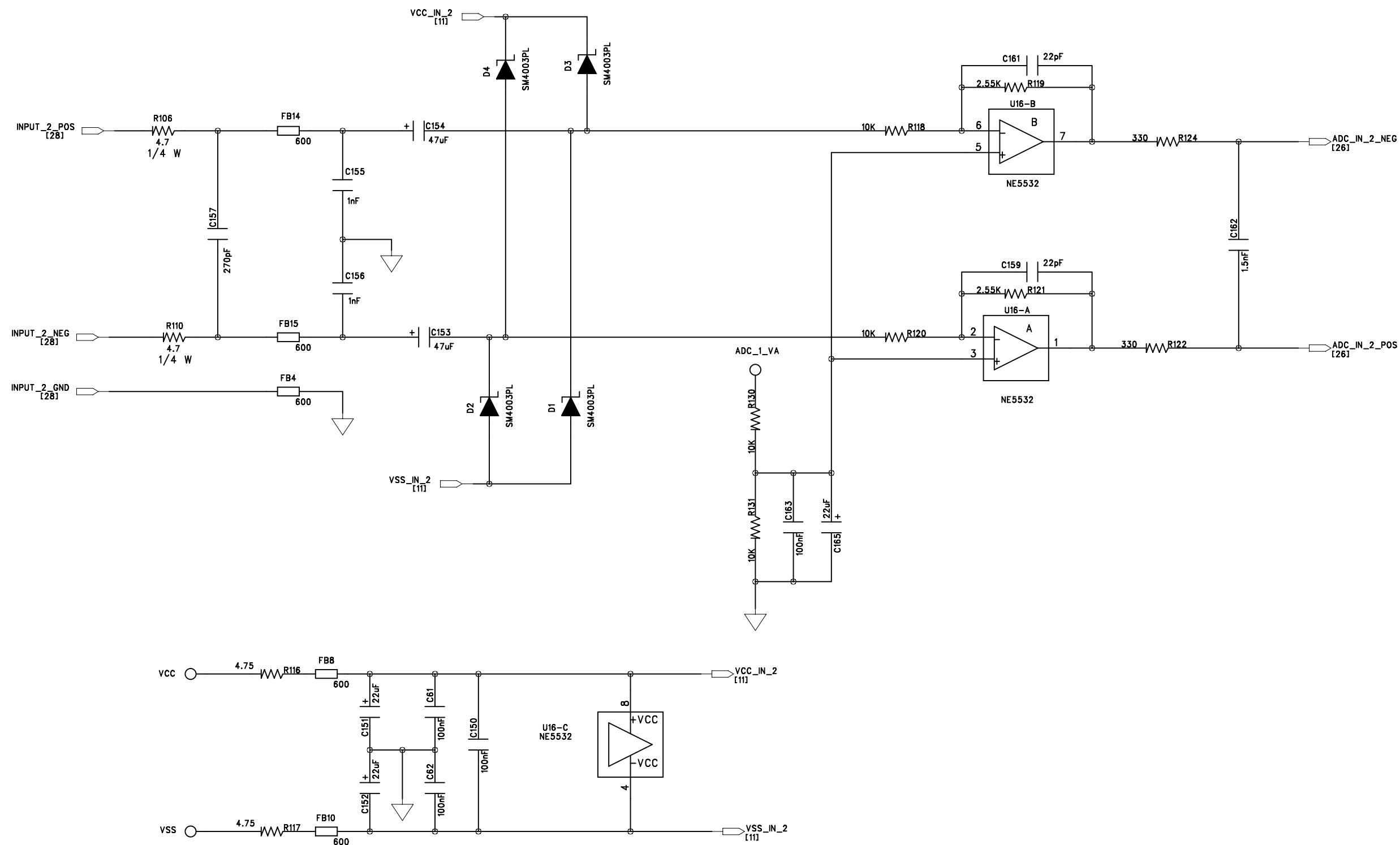


FPGA VINT 1.2V Supply





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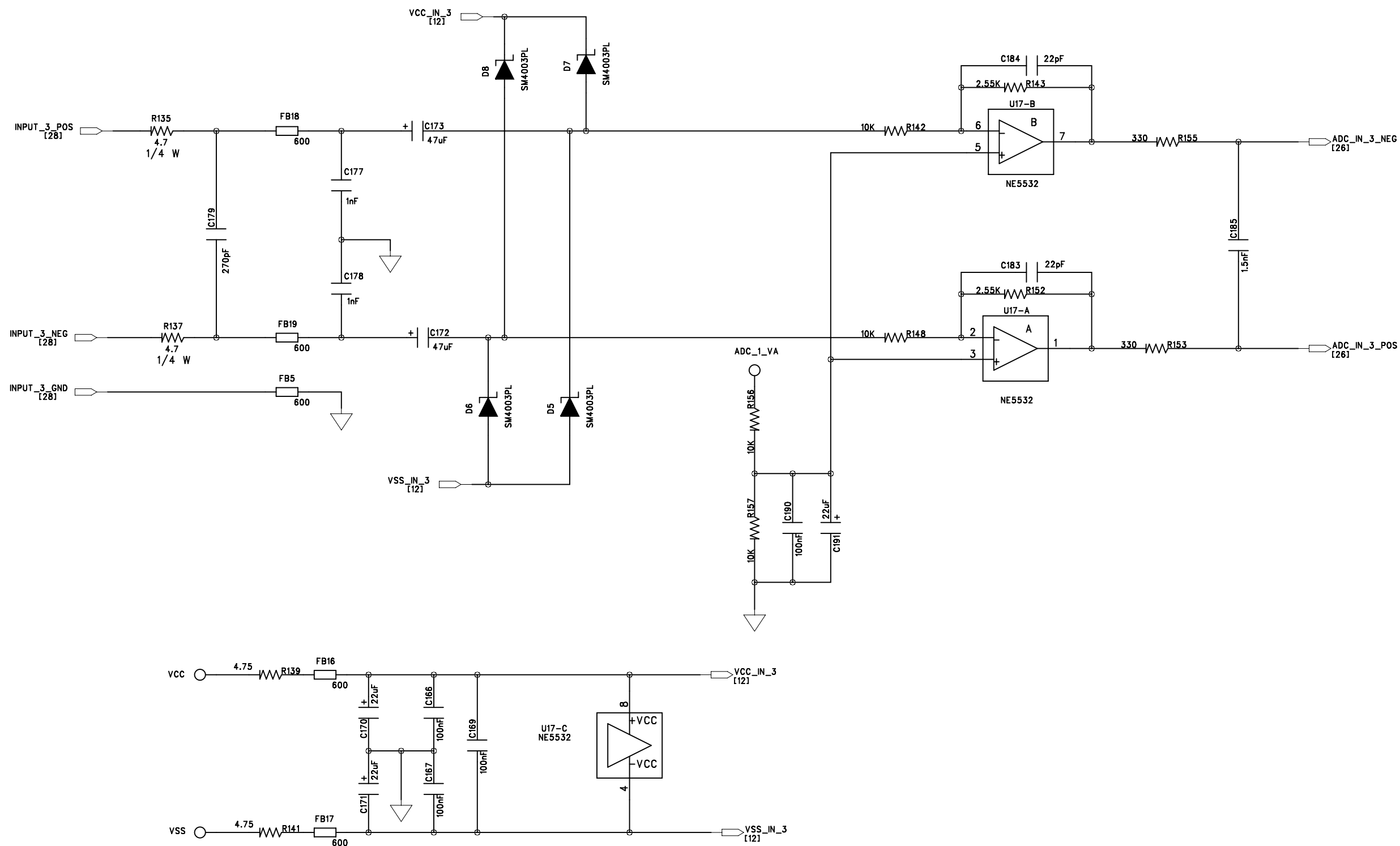
INPUT_2 <undefined>

REV. - 4.0

Drawn By: RIK

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LEX-16L 4 0.sch

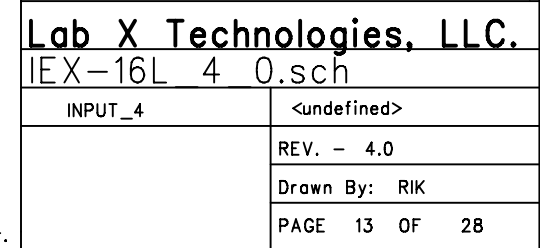
INPUT_3 <undefined>

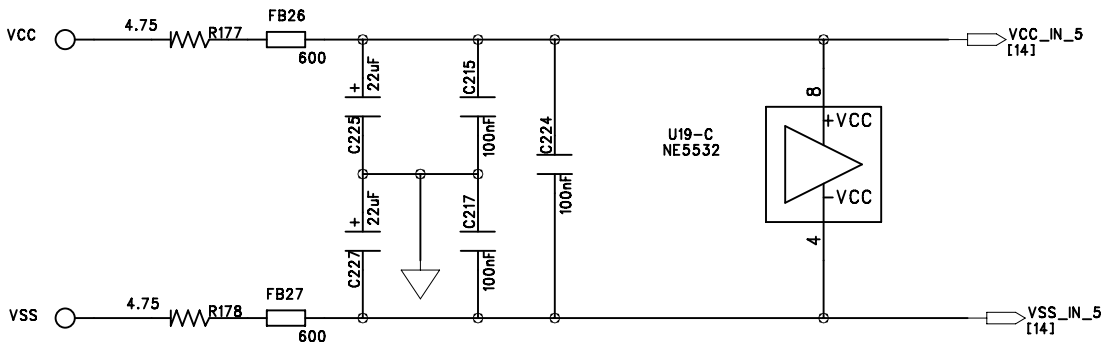
REV. - 4.0

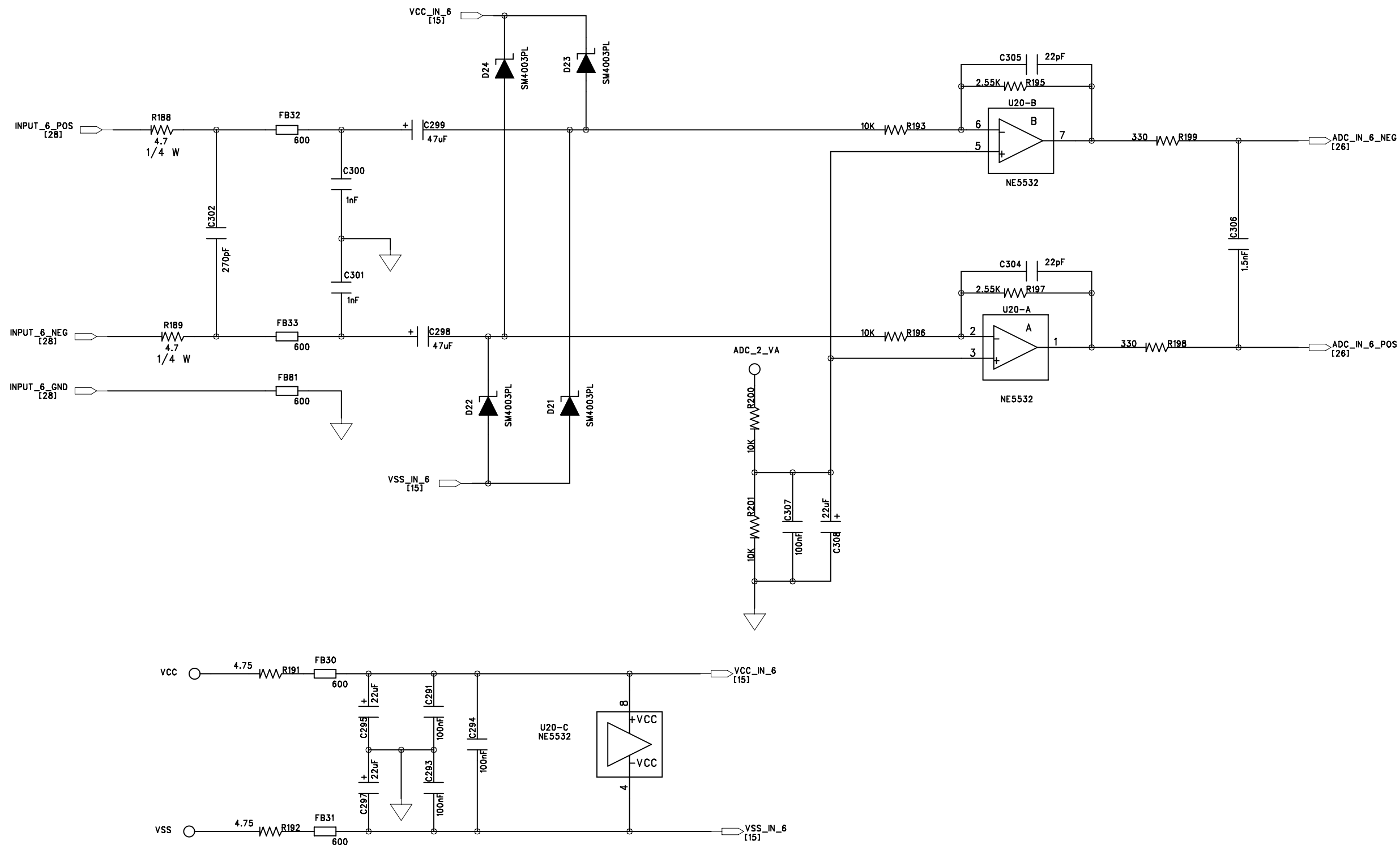
Drawn By: RIK

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IEX-16L 4 0.sch

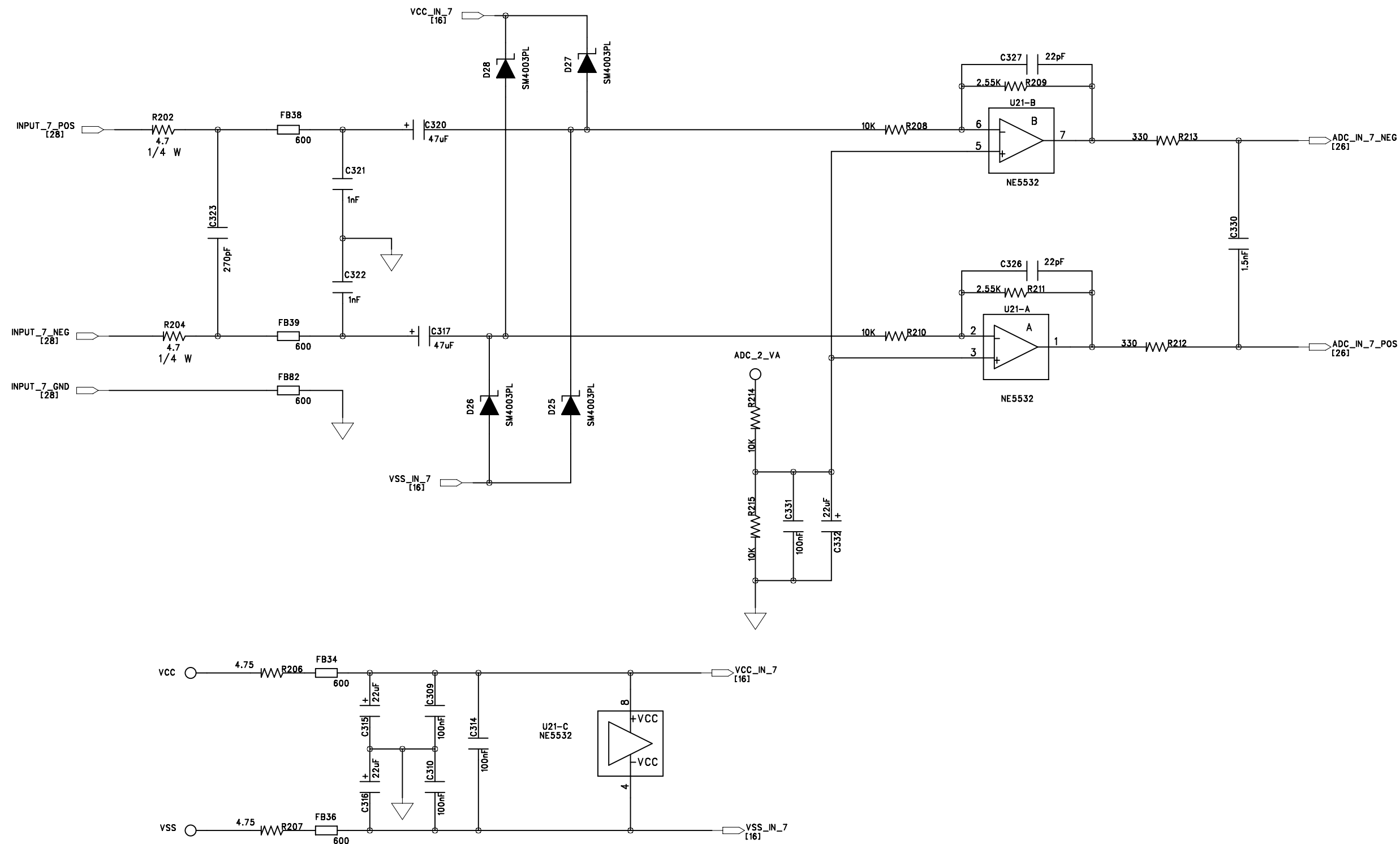
INPUT_6 <undefined>

REV. - 4.0

Drawn By: RIK

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LEX-16L 4 0.sch

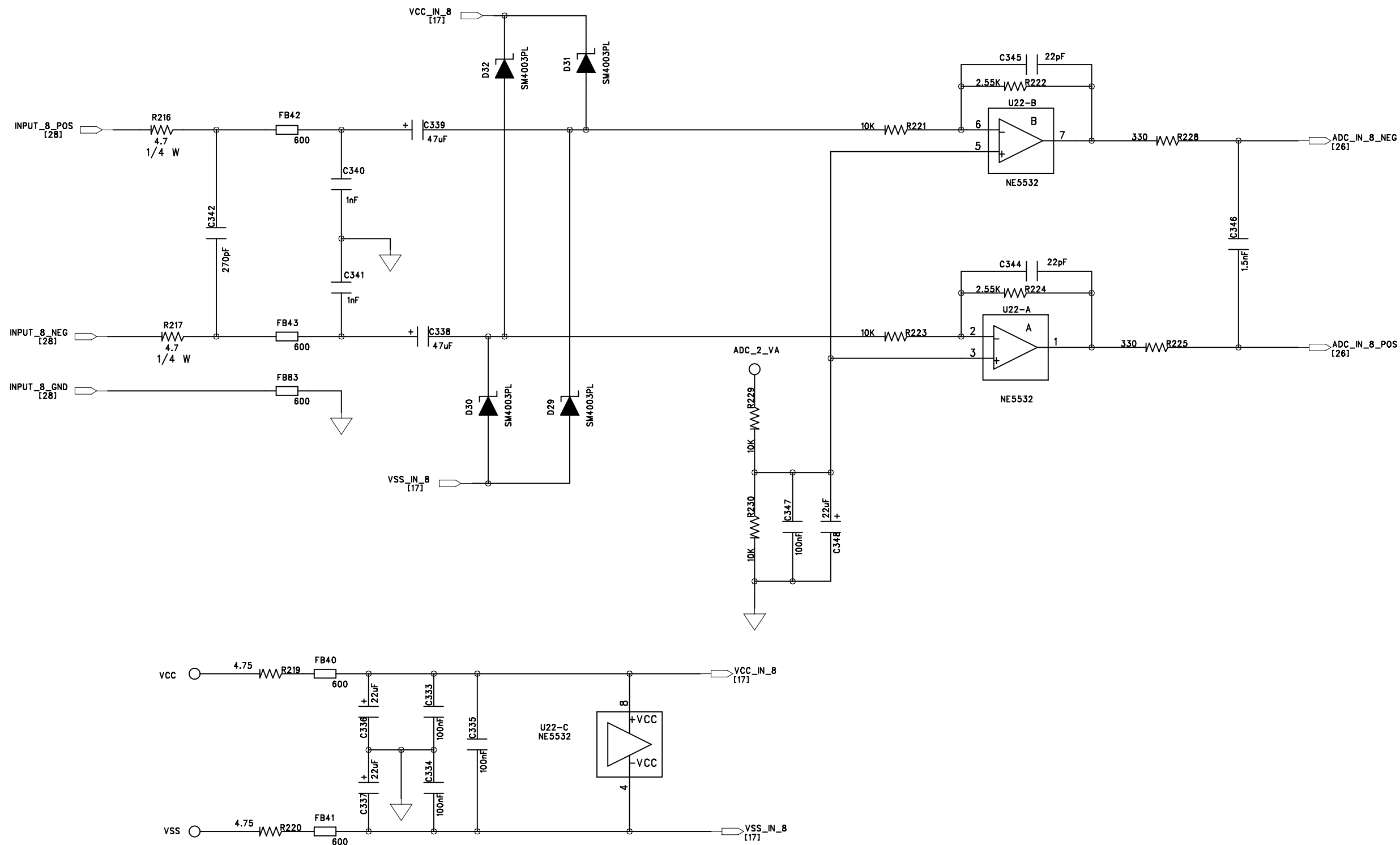
INPUT_7 <undefined>

REV. - 4.0

Drawn By: RIK

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IEX-16L 4 0.sch

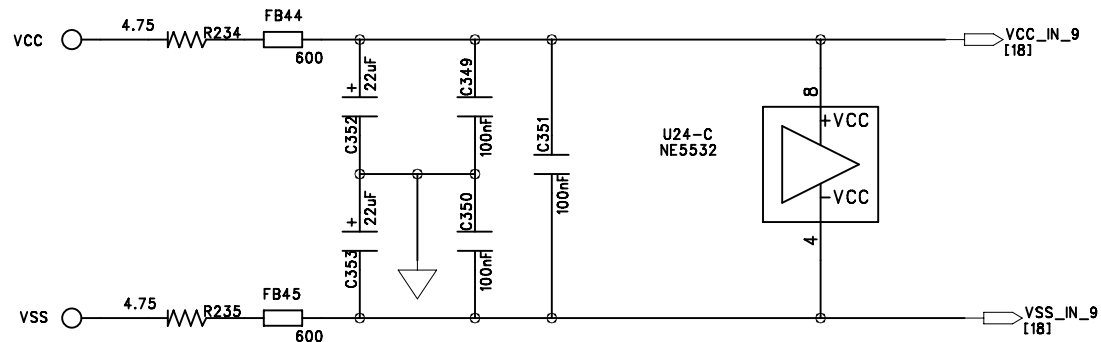
INPUT_8 <undefined>

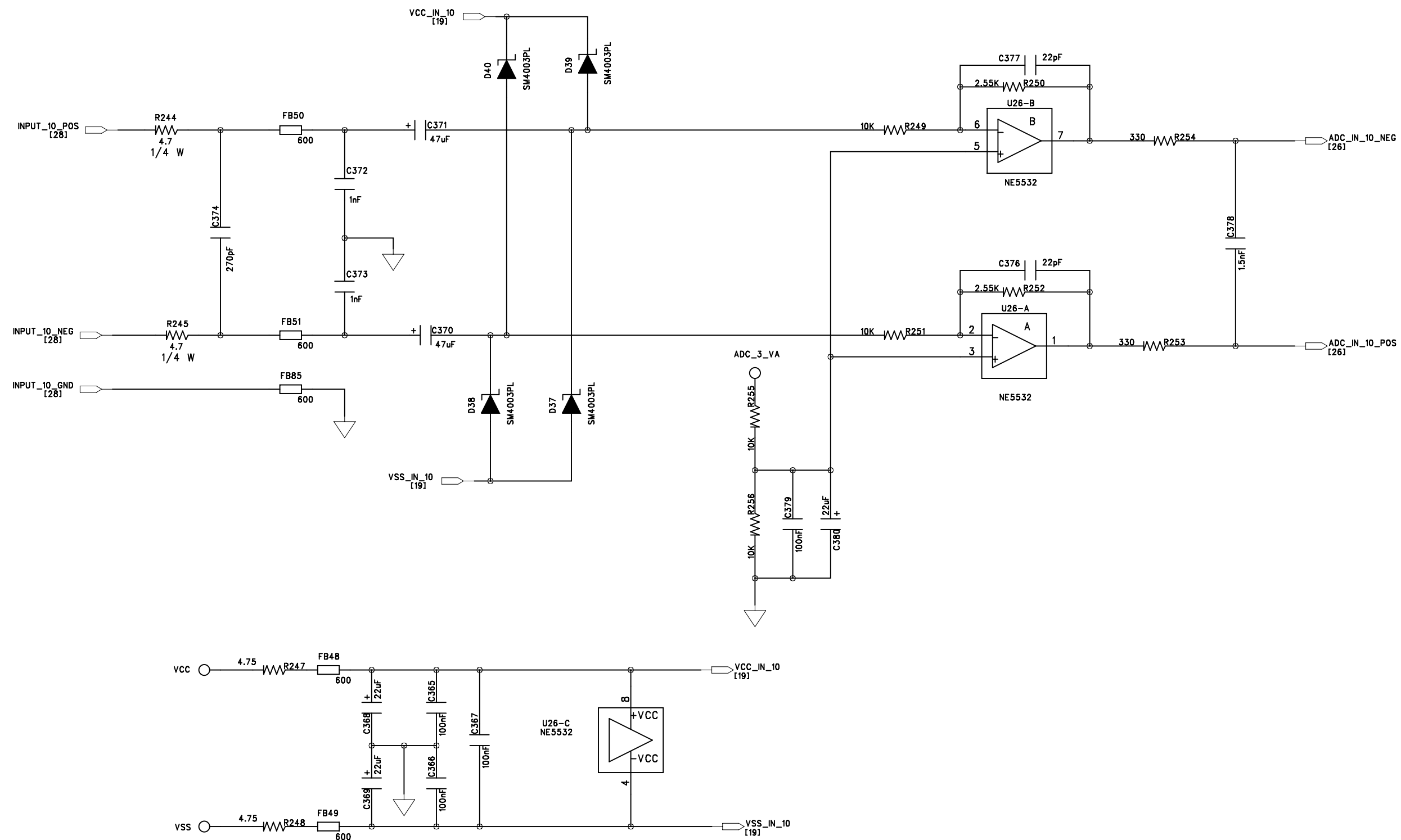
REV. - 4.0

Drawn By: RIK

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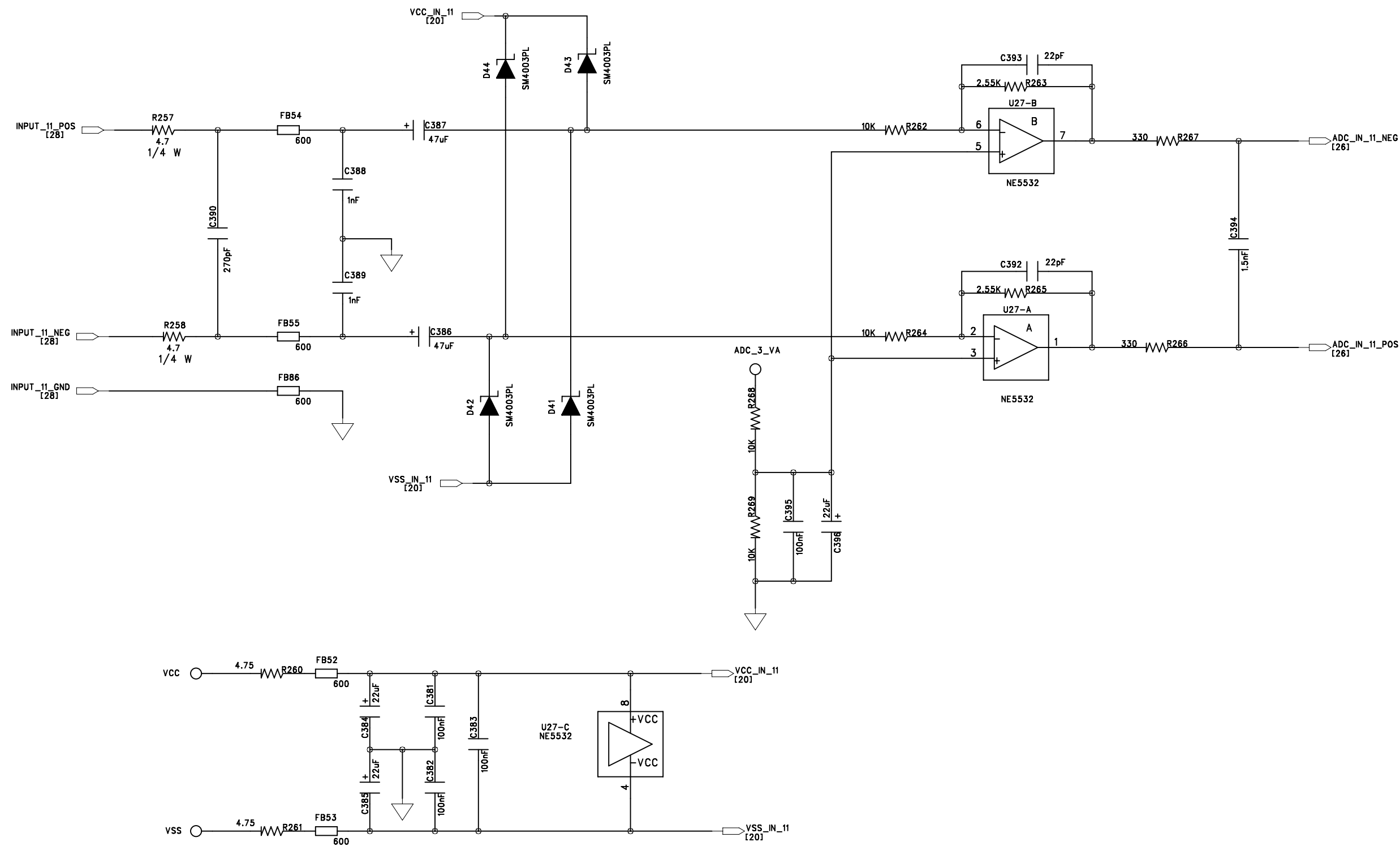
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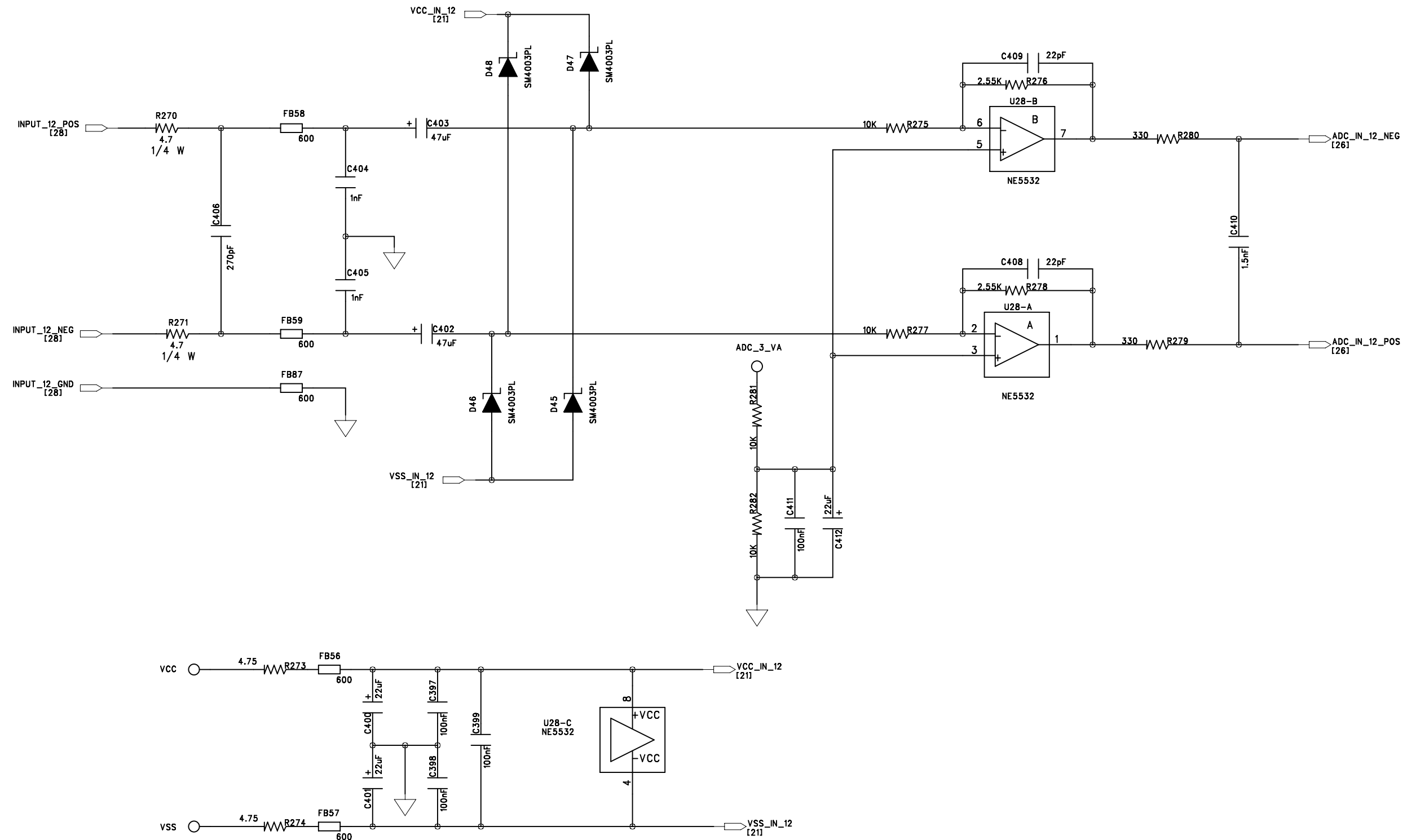
Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
INPUT_10	<undefined>
	REV. - 4.0
	Drawn By: RIK
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Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
INPUT_11	<undefined>
	REV. - 4.0
	Drawn By: RIK
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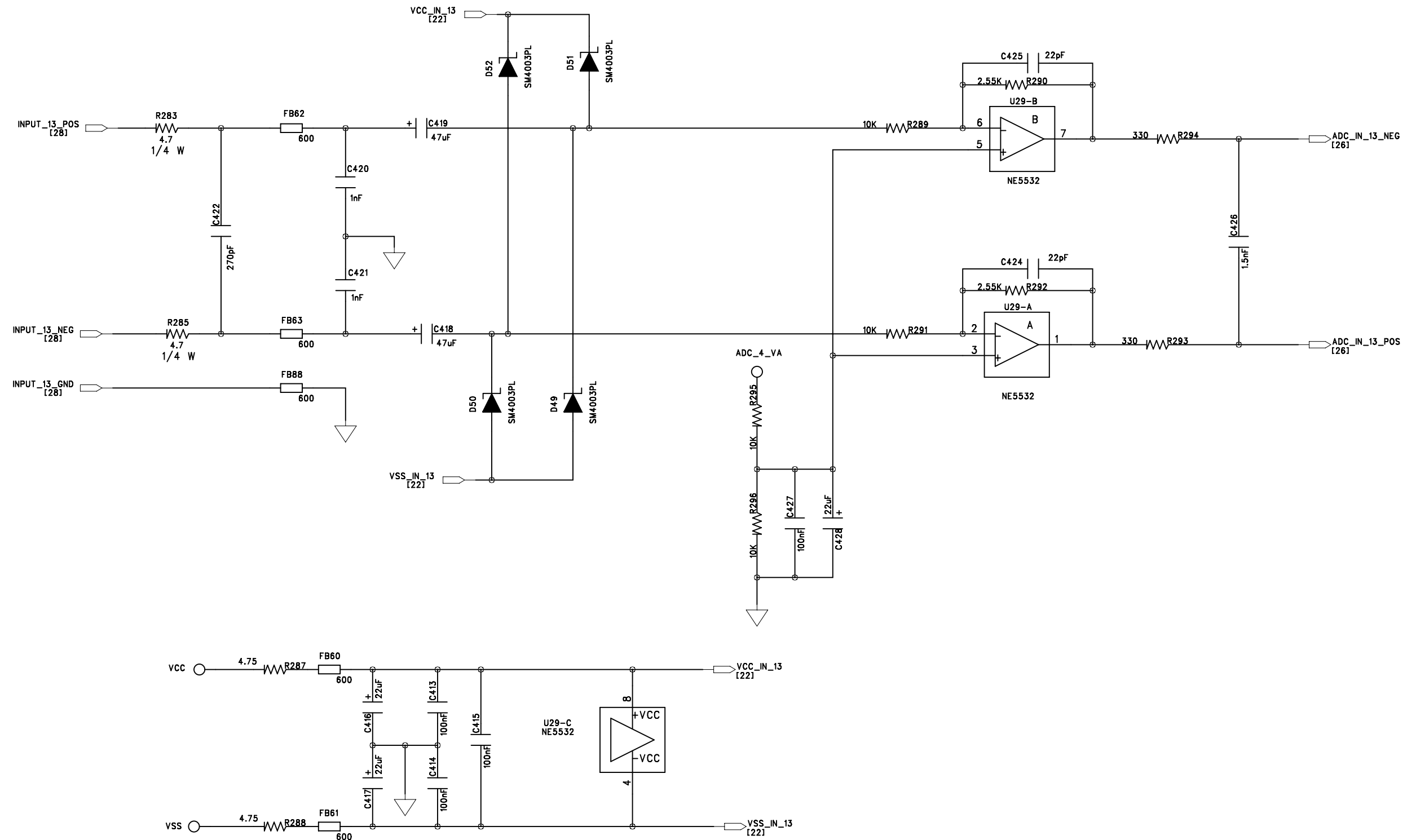


Lab X Technologies, LLC.

LEX-16L 4 0.sch

INPUT_12	<undefined>
REV. - 4.0	
Drawn By: RIK	
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LEX-16L 4 0.sch

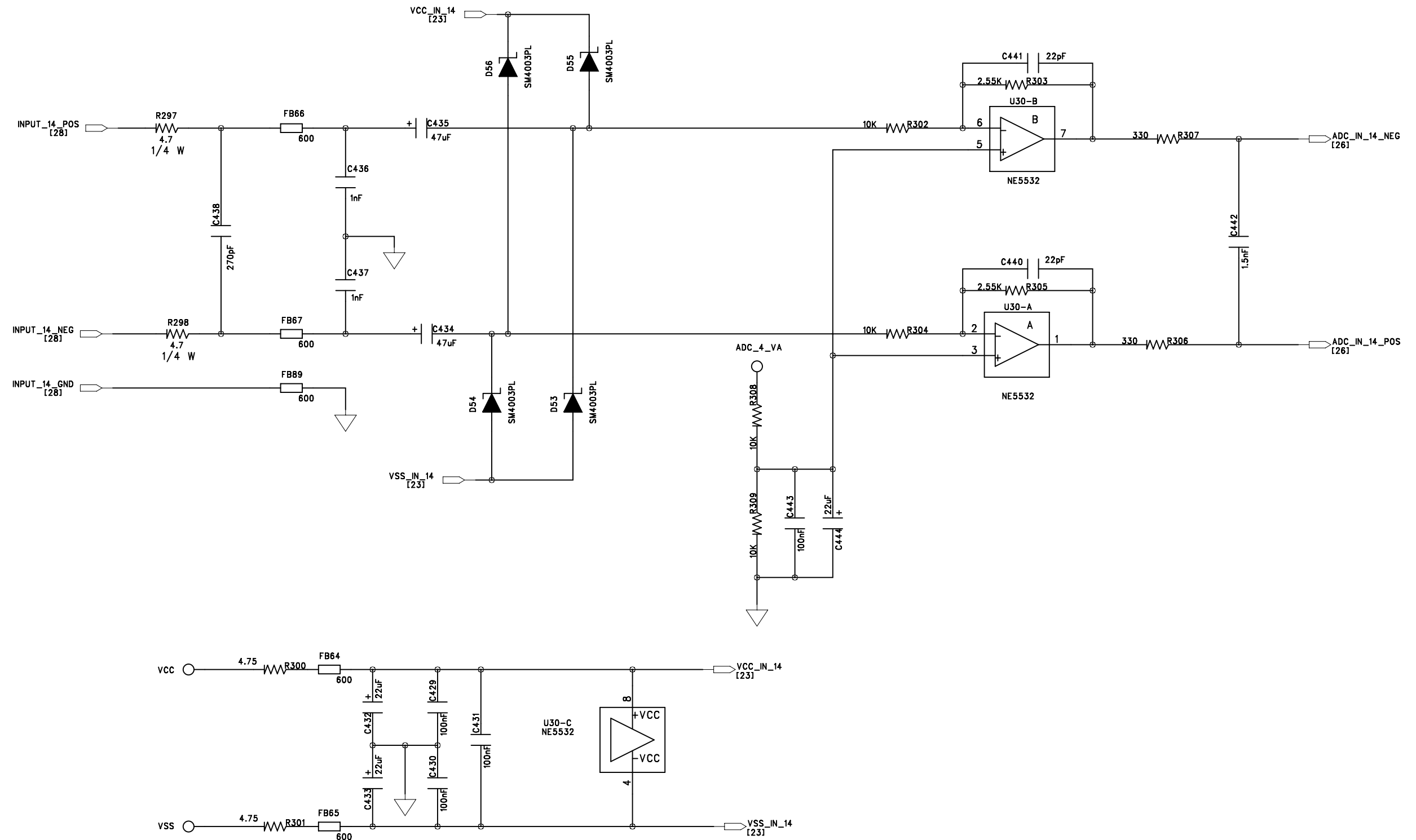
INPUT_13 <undefined>

REV. - 4.0

Drawn By: RIK

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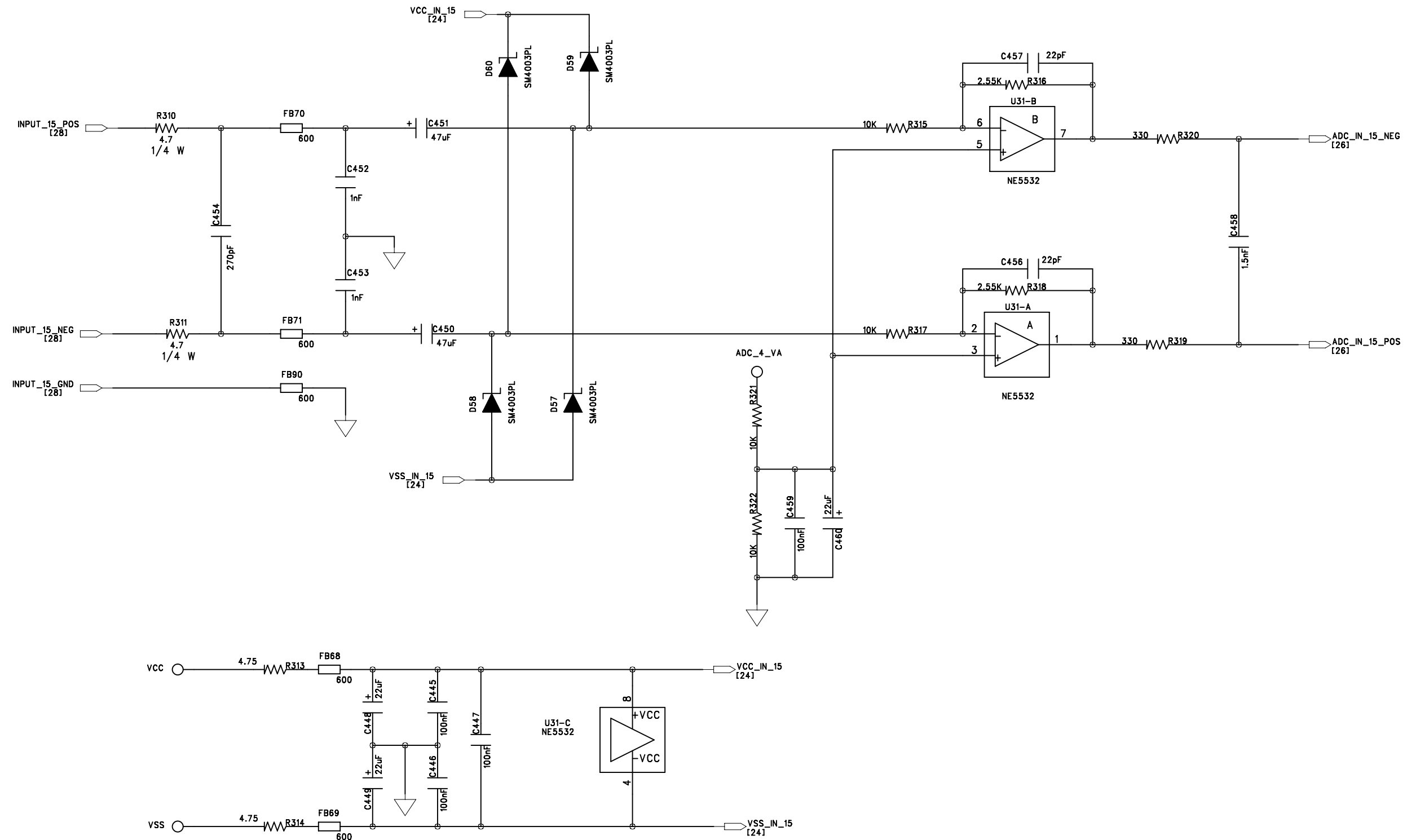


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IEX-16L 4 0.sch

INPUT_14	<undefined>
REV. - 4.0	
Drawn By: RIK	
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IEX-16L 4 0.sch

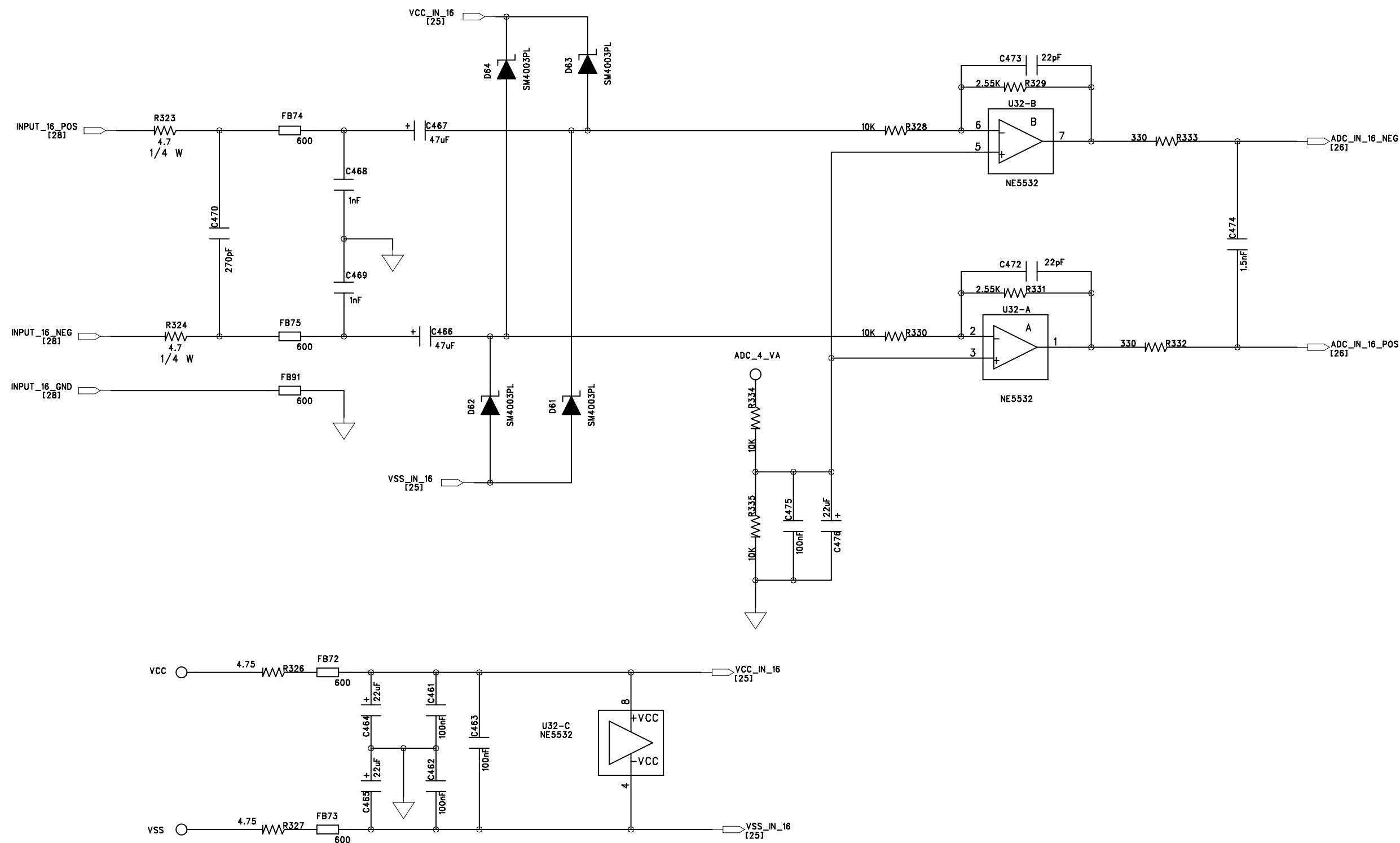
INPUT_15 <undefined>

REV. - 4.0

Drawn By: RIK

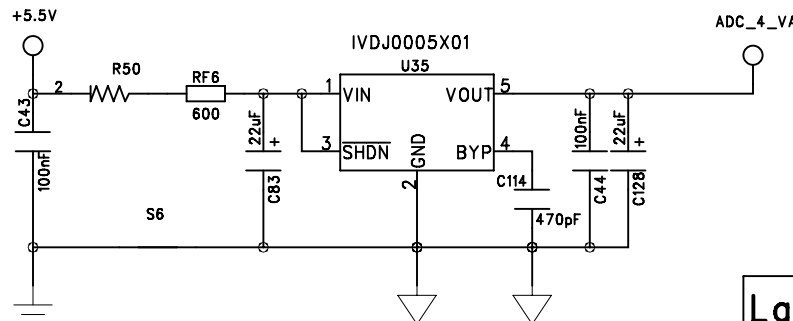
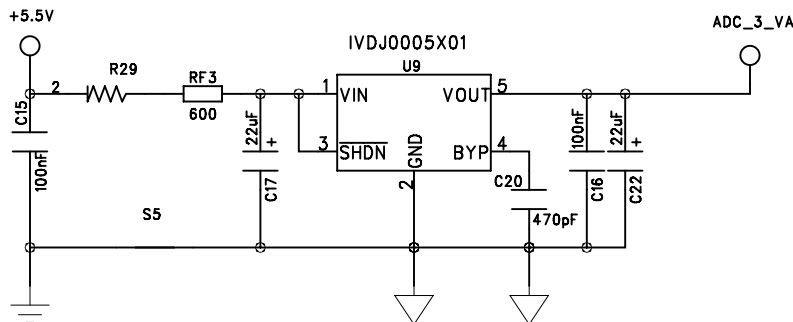
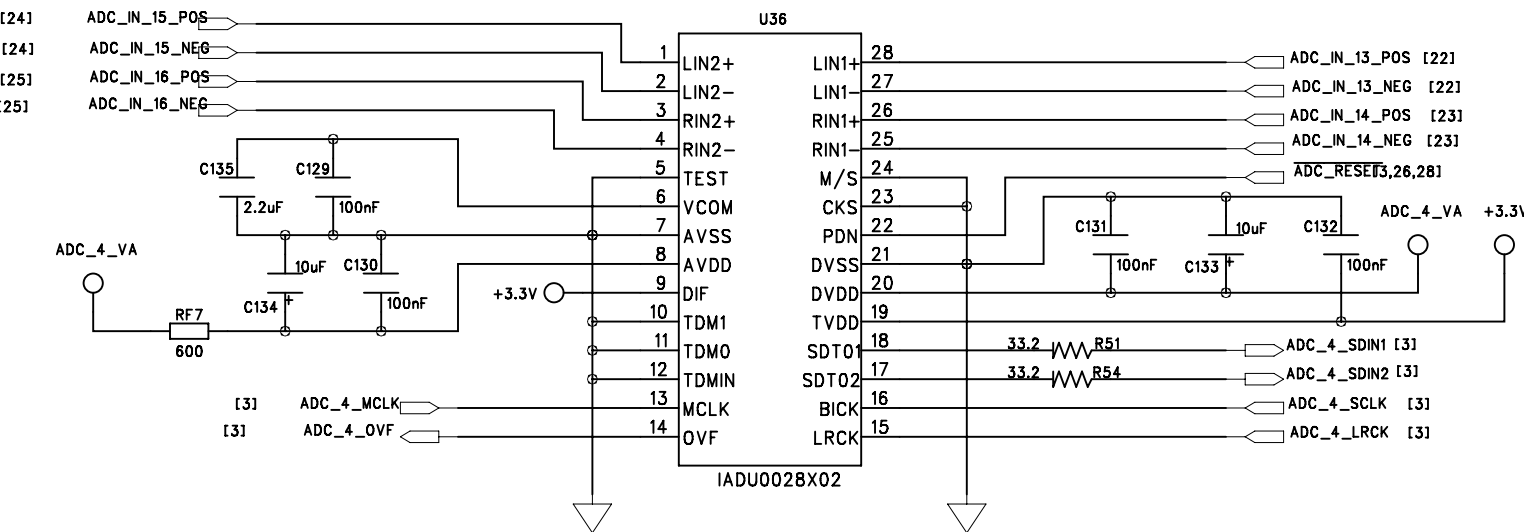
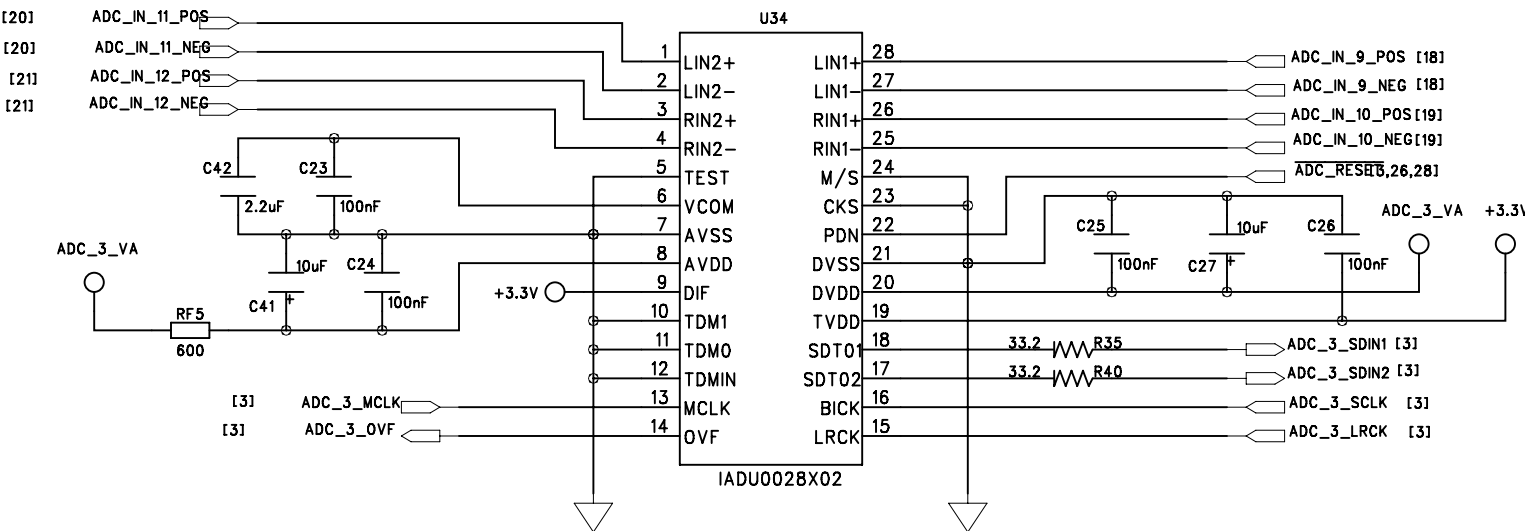
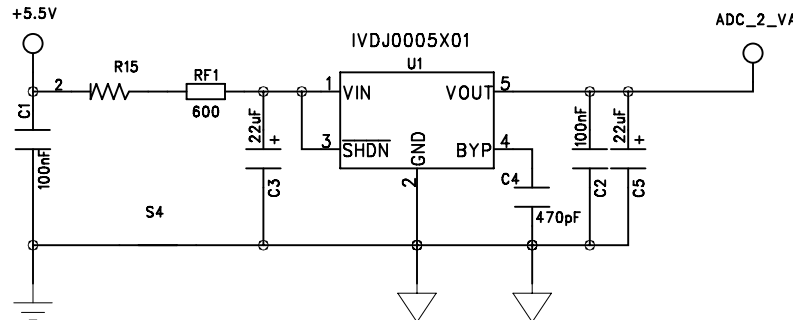
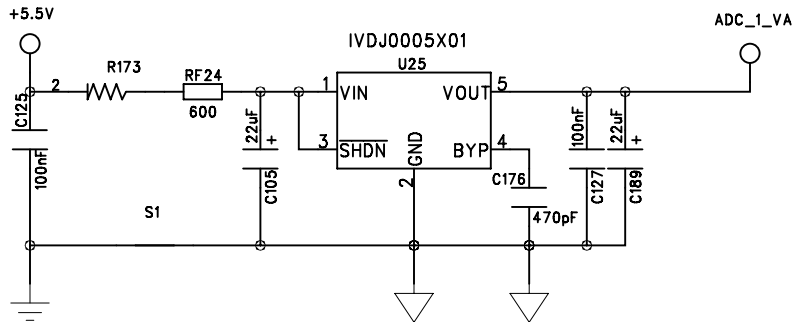
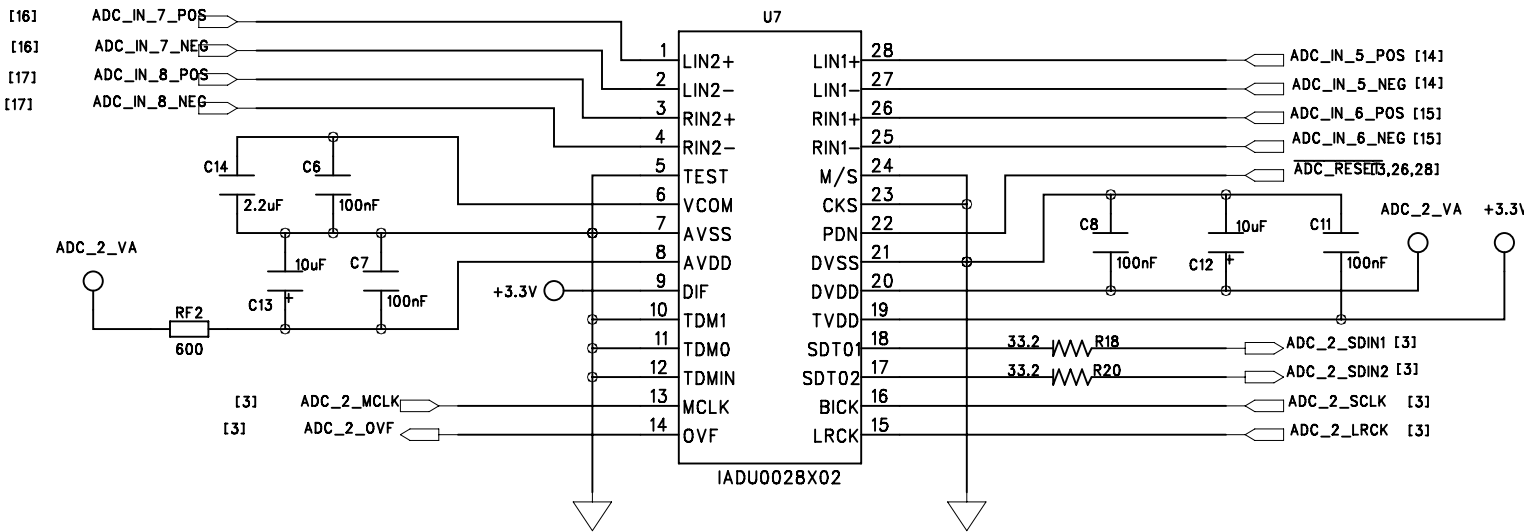
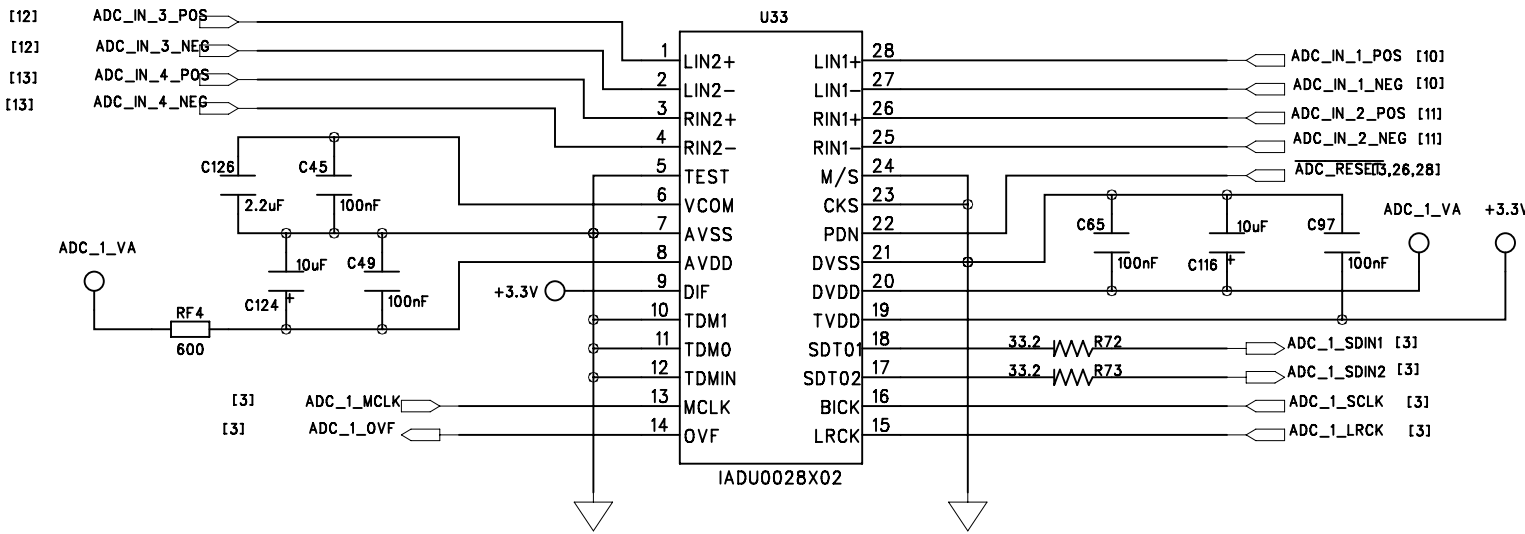
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Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
INPUT_16	<undefined>
REV. - 4.0	
Drawn By: RIK	
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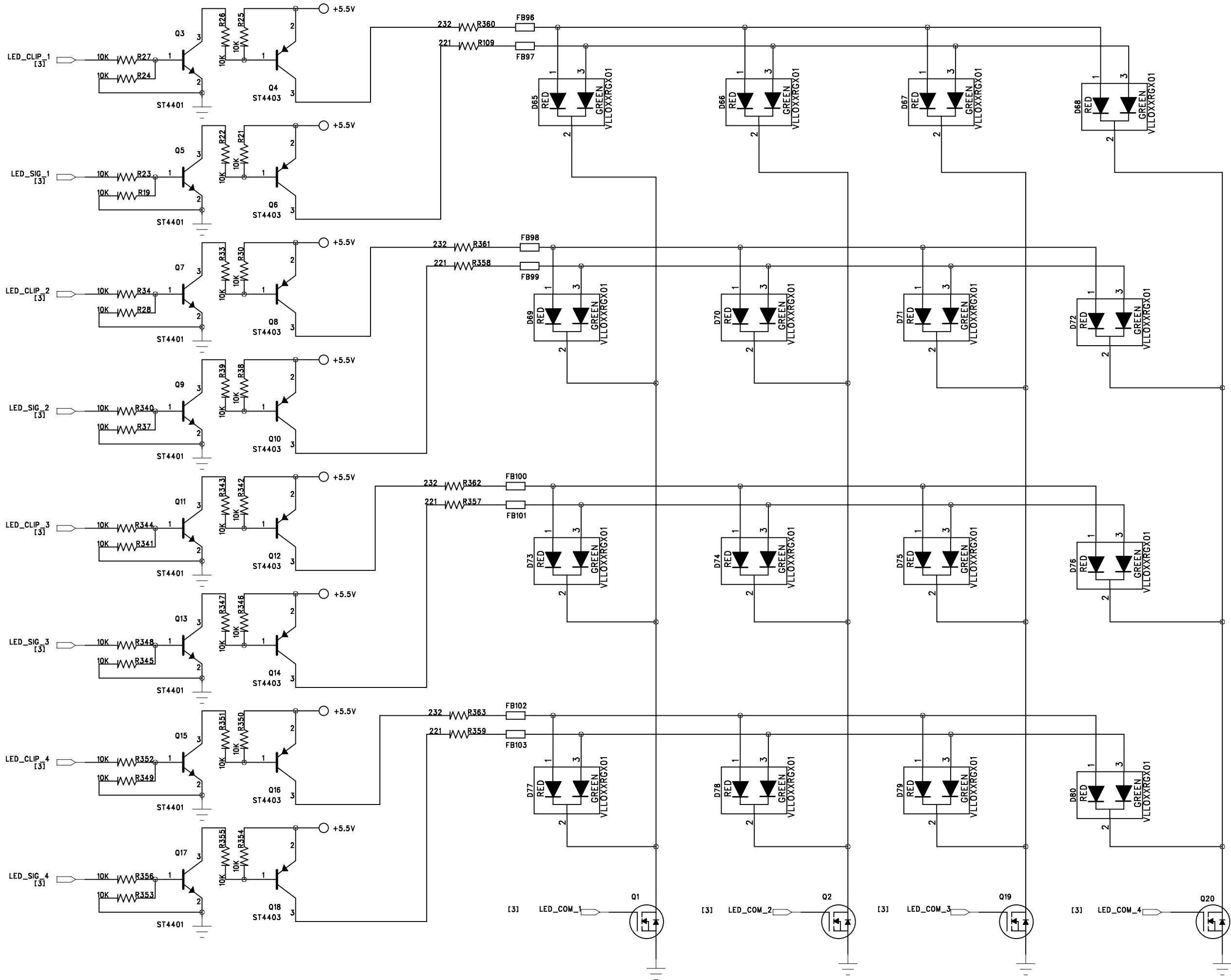


Lab X Technologies, LLC.

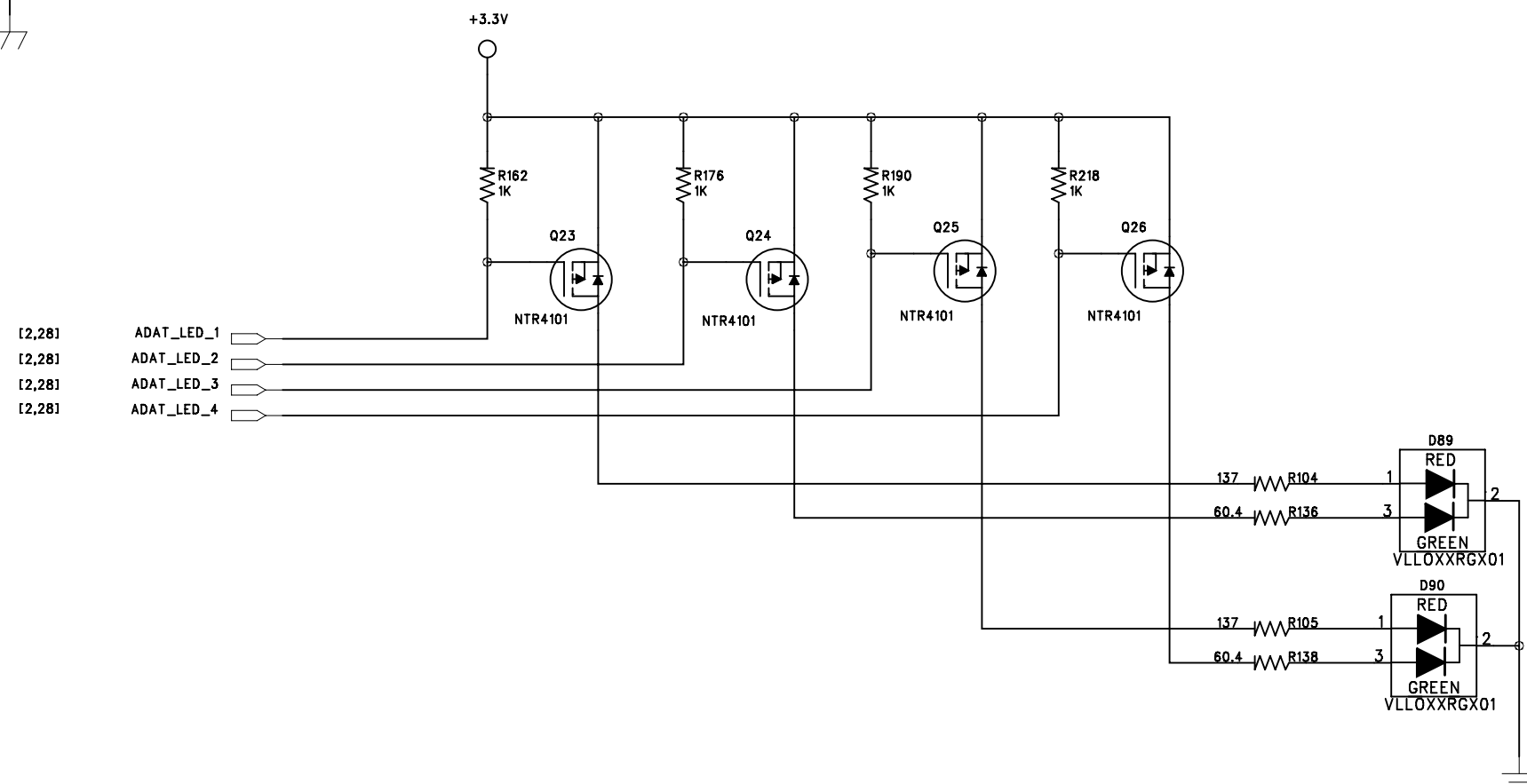
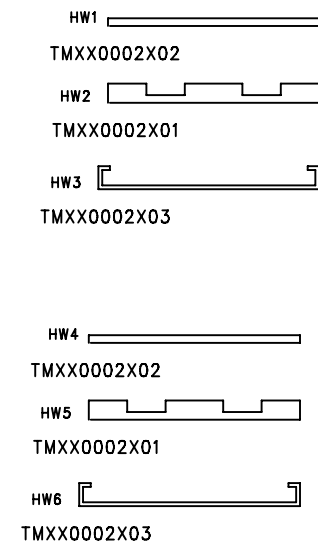
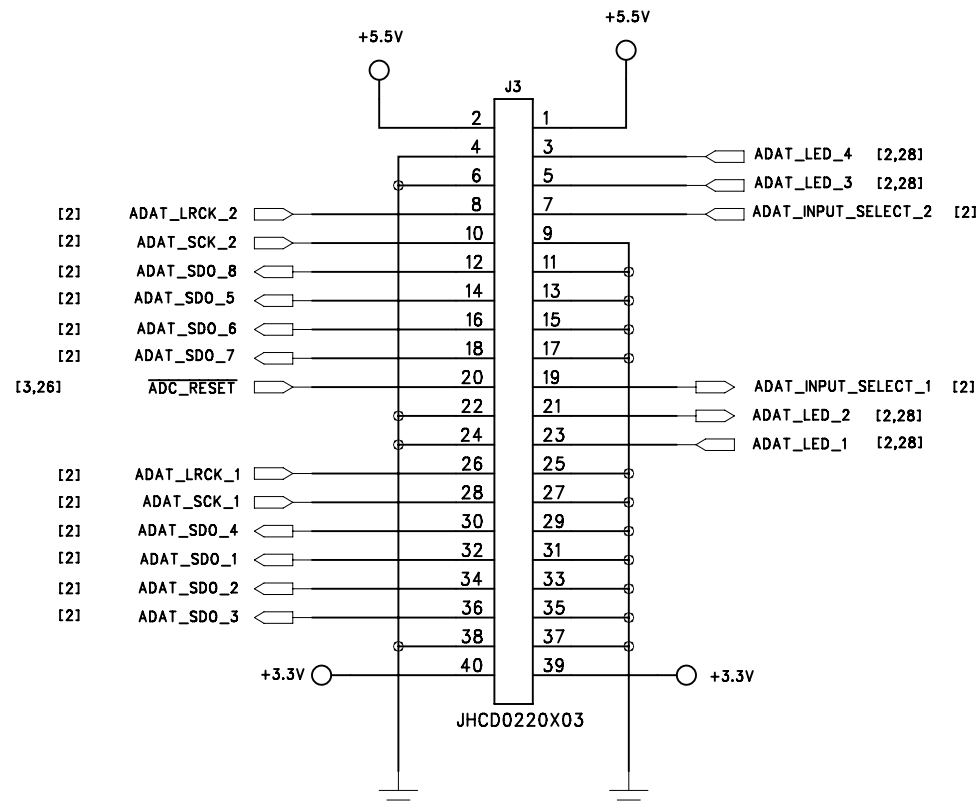
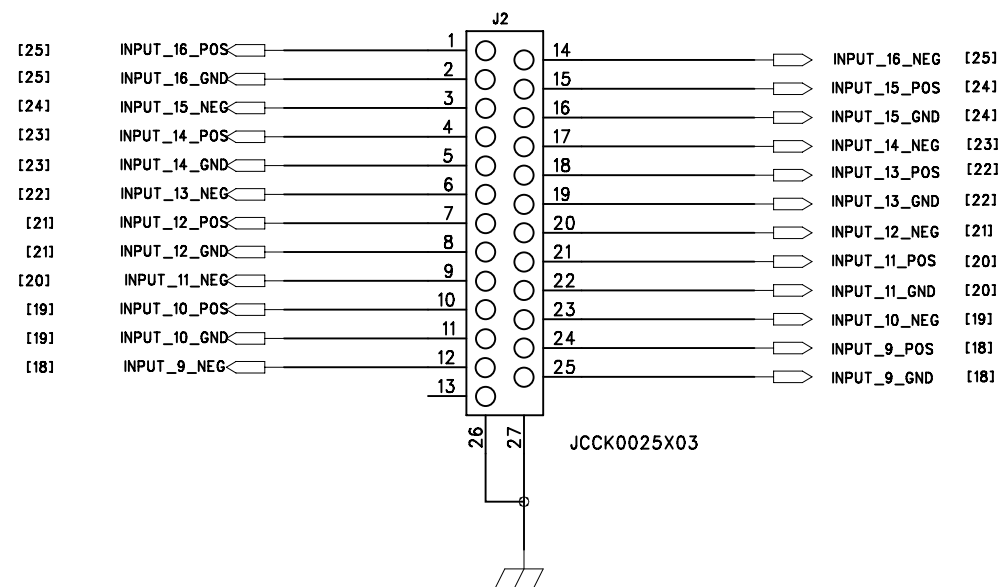
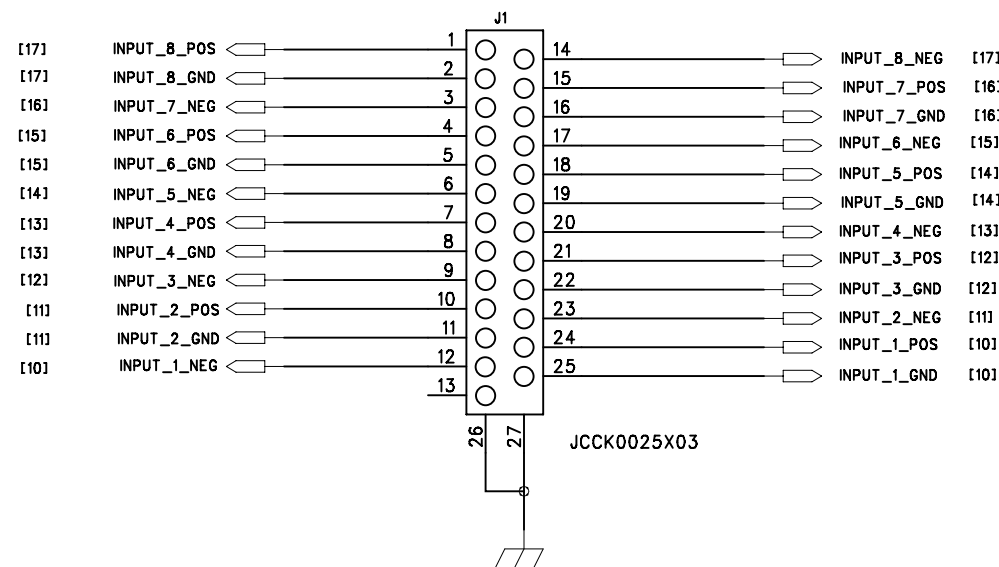
IEX-16L 4 0.sch

ADC	<undefined>
REV.	- 4.0
Drawn By:	RIK
PAGE	26 OF 28

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Lab X Technologies, LLC.	
IEX-16L 4 0.sch	
EXTRA	<undefined>
	REV. - 4.0
	Drawn By: RIK
	PAGE 28 OF 28